STA summary

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1. **STA:**
    a. **delay calculation considering PVT corners:**
        i. cell delay && net delay
        ii. crosstalk delta delay
        iii. clock uncertainty
        iv. clock latency
        v. clock recovery
        vi. CRPR
        vii. derating delay for OCV by PVT variation

    b. define appropriate SDC:
        i. one-cycle path
        ii. multicycle path
        iii. false path
        iv. set_disable_timing
        v. half-cycle path
        vi. time across clock domain
        vii. multiple clock
        viii. data to data
        ix. clock gating

    c. obtain slack by setup check && hold check

2. **Tlaunch && Tcapture** (the appropriate time for setup check && hold check) by:
    a. one-cycle path
    b. multicycle path
        i. set_multicycle_path 3 -setup \
           -from [get_pins UFF0/Q] \
           -to [get_pins UFF1/D]
    c. half-cycle path
        i. to relax hold check
    d. timing across clock domain
        i. set_multicycle_path 4 -setup \
           -from [get_clocks CLKM] -to [get_clocks CLKP] **-end**
    e. multiple clock
        i. integer multiple
        ii. non-integer multiple
        iii. Phase-shift

3. **Cell delay by Timing Arcs in Timing Library**
    a. Combinational logic (e.g. inverter cell):
        i. [input transition, output load cap] in 2D-timing model
    b. Sequential logic (from CLK to Q):
        i. [clock transition, output load cap] in 2D-timing model

4. **Setup time && Hold time Constraints in Timing Library**
    a. Sequential logic (from CLK to D):
        i. [clock transition, data transition] in 2D-timing model

5. **Max delay for setup check**: max{Tlaunch + Tco + Tdata} > Tcapture + Tcycle -

Tsetup
   a. Normally a Tcycle slack

6. **Min delay for hold check**: min{Tlaunch + Tco + Tdata} < Tcapture + Thold
   a. For capture path, hold check is a Tcycle prior to setup check by default
   b. Use set_multicycle_path to define the time for setup check && hold check in launch path && capture path

7. **Length in wireload model due to interconnect parasitics**
   a. Decided by fanout
   b. Derive R: length * R_coeff
   c. Derive C: length * C_coeff
   d. Derive Area: length * area_coeff

8. **Clock**
   a. **Clock Uncertainty:**
      i. clock skew: difference in timing between two or more signals, maybe data, clock or both
      ii. clock jitter
      iii. another pessimism
      iv. usage: set_clock_uncertainty 0.250 -setup [get_clocks BZCLK]
   b. **Clock Latency:**
      i. clock latency: total time from clock source to an end point
      ii. usage: set_clock_latency 2.2 [get_clocks BZCLK]

9. **SI: Crosstalk and Noise**
   a. **Glitch:**
      i. refers to noise caused on a steady victim signal due to coupling of switching activity of neighboring aggressors
   b. **Crosstalk delta delay**
      i. by coupling of switching activity of the victim with the switching activity of the aggressors
      ii. positive delta delay > forward in time > late
      iii. negative delta delay> backward in time > early

10. **Timing Path Groups**
    a. Timing paths are sorted into path groups by the clock associated with the endpoint of the path.

    b. create_clock: to create a master clock.
       i. set_clock_transition: to specify the slew at the source of the clock.

    c. create_generated_clock: to create a clock derived from a master clock.

    d. virtual clock
       i. used as a reference in STA analysis to specify input and output delays relative to a clock.
       ii. used along with set_input_delay and set_output_delay.

    a. create_clock, set_input_delay (constrain input path) and set_output_delay (constrain output path) is enough to constrain four kinds of timing paths:
       i. Input port to output port
       ii. Input port to D pin
       iii. Clock pin to D pin
       iv. Clock pin to output port

11. **Timing in I/O pin**
    a. input:
        i. set_drive
        ii. set_driving_cell
        iii. set_input_transition
    b. output:
        i. set_load

12. **Design Rule Checks**
    a. set_max_transition
    b. set_max_capacitance
        i. The capacitance on a net is calculated by taking the sum of all the pin capacitances
        plus any IO load plus any interconnect capacitance on the net.
    c. set_max_fanout (for synthesis)
    d. set_max_area (for synthesis)

13. **Timing Analysis Refine**
    a. set_case_analysis: to define the constant signals
    b. set_disable_timing: to break the timing arc
    c. set_false_path: to define the timing paths that are not real (e.g. from one clock domain to another clock domain)

14. **On chip variation (OCV)**
    a. the PVT on single die affect the distribution of cell delay and wire delay.
    b. setup check in OCV (SS):
        i. set_timing_derate -early 0.8 #-early: capture path
        ii. set_timing_derate -late 1.1 #-late: launch path
    c. hold check in OCV (FF):
        i. set_timing_derate -early 0.9 #-early: launch path
        ii. set_timing_derate -late 1.2 #-late: capture path
    d. Clock Reconvergence Pessimism Removal (CRPR):
        i. CPP itself is the delay difference along this common portion of the clock tree due to different deratings for launch and capture clock paths.

15. **Time borrowing**
    a. Latch, opening edge, closing edge
    b. Time borrowed from end point
        i. No time borrowing: slack over 0
        ii. Time borrowing: slack equal to 0

16. **Data to Data Check**
    a. setup check: zero-cycle check
        i. usage: set_data_check -from SDA (related pin) -to SCTRL (constrained pin) -setup 2.1
    b. hold check: a Tcycle prior to setup check at the capture edge
        i. usage: set_multicycle_path -1 -hold -to UAND0/A2

17. **Clock Gating**
    a. active-high clock gating
        i. When gating signal is 1 (active-high), [AND or NAND] cell can

generate clock signal of 1.
   ii. Usage: set_clock_gating_check -high [get_cells UMUX0]
   iii. Gating signal changes when clock signal of 0.
   iv. for hold check, use inverter to delay launch path
b. active-low clock gating
   i. When gating signal is 0 (active-low), [OR or NOR] cell can produce clock signal of 0.
   ii. Gating signal changes when clock signal of 1.
c. ICG: latch combined with gating cell
   i. latch: to align the edge of gating signal with the edge of clock signal to generate the gating signal that satisfies setup check and hold check