

Synopsys TCL

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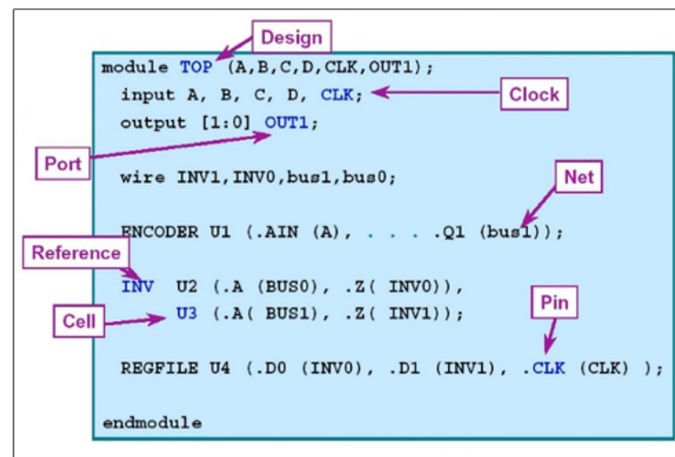
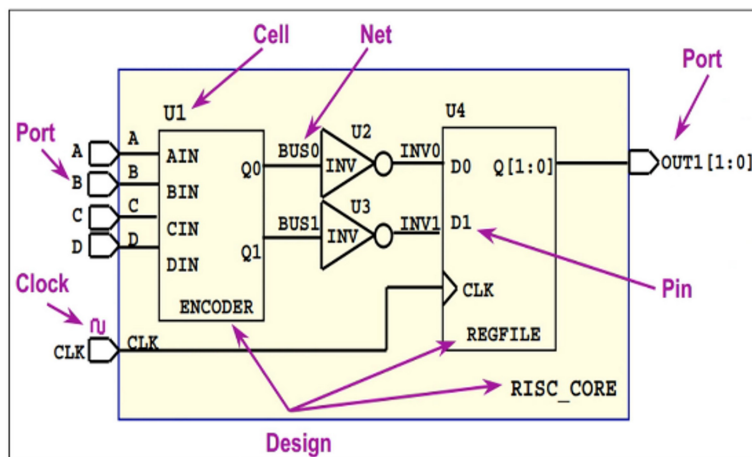
Synopsys TCL

application commands: provided by Synopsys tool, written as a command procedure in C or C++, using TCL extension mechanism

sizeof_collection [all_clocks]

TCL的应用：Design Object

通过对Design Object的分析，我们来了解和学习DC获取电路并进行解析的方法。



Schematic View and Code of Design Objects

get_ports portsName #返回design中对应的ports object

example:

```
get_ports CLK
{CLK}
```

get_ports * ##通配符*表示all

```
{A B C D CLK OUT[0] OUT[1]}
```

get_ports C* ##获取C开头的port

```
{CLK}
```

cell: ref_name, instance_name

ref_name: 例化的实例，比如encoder, regfile

instance_name:

```
{U1 U2 U3 U4}
```

reference是唯一的，但如果存在多个reference，贴上instance name区分

get_cells cellsName #返回design中cell的instance name object

example:

```
get_cells U4 #get_cells获得instance name
{U4}
```

get_cells * #获得所有的cell的instance name

```
{U1 U2 U3 U4}
```

get_cells *3 #加入通配符*来表示3结尾的instance name

```
{U3}
```

get_nets netsName #返回design中net的object

example:

```
get_nets INV*
{INV0 INV1}
```

get_nets *

```
{A B C D CLK BUS0 BUS1 INV0 INV 1 OUT[0] OUT[1]}
```

sizeof_collection [get_nets *]

```
11
```

get_pins pinsName #返回design中pin的object

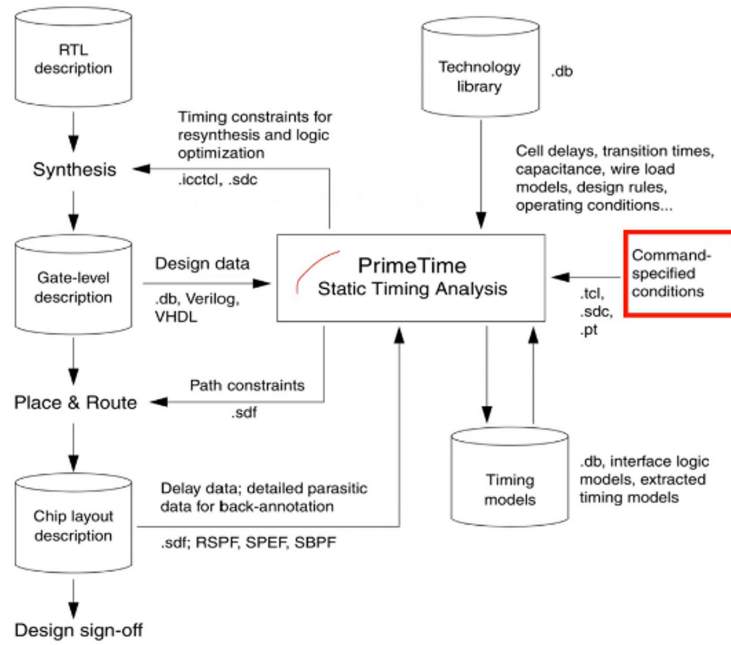
example:

get_pins */Z #查看design里哪些pin的名字叫做Z，每一个引脚固定有/说明所在的单元
{INV0/Z INV1/Z}

get_pins */Q* #查看design里哪些pin的名字以Q开头
{ENCODER/Q0 ENCODER/Q1 REGFILE/Q[1] REGFILE/Q[0]}

PT:

01-PrimeTime



lib: tech lib && timing models

1. 时序库和时序模型怎么计算delay
2. PR和综合阶段如何进行静态时序分析以满足要求
3. Based on Tcl environment