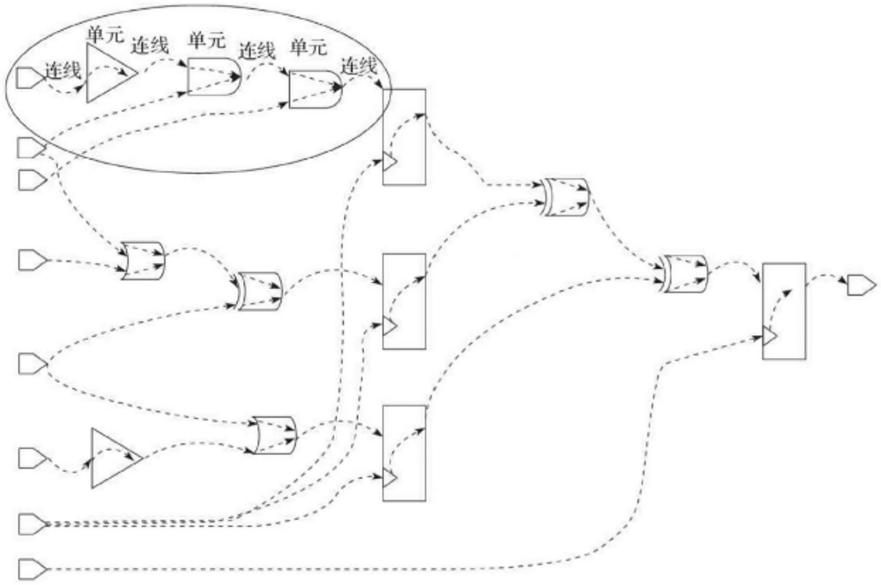
STA concepts

2022年6月9日　　13:59

STA concepts

Timing Arc >>> 描述延时 >>> 连线延时 + 单元延时

Timing Arc

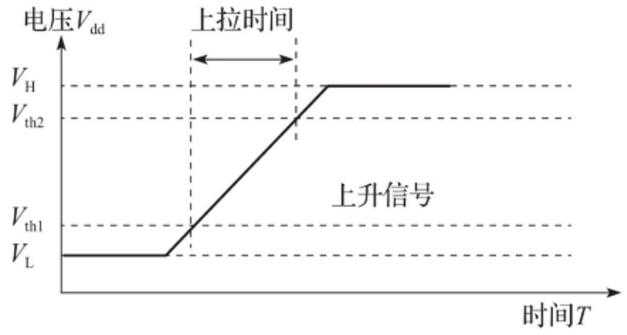


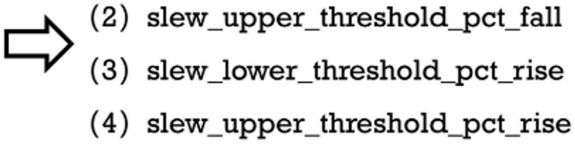
net delay和cell delay
cell delay
transition delay from 0 to 1 || from 1 to 0
slew rate压摆率定义电压转换速率

1. slew_lower_threshold_pct_fall
2. slew_upper_threshold_pct_fall
3. slew_lower_threshold_pct_rise
4. slew_upper_threshold_pct_rise

Cell delay

(1) Transition delay



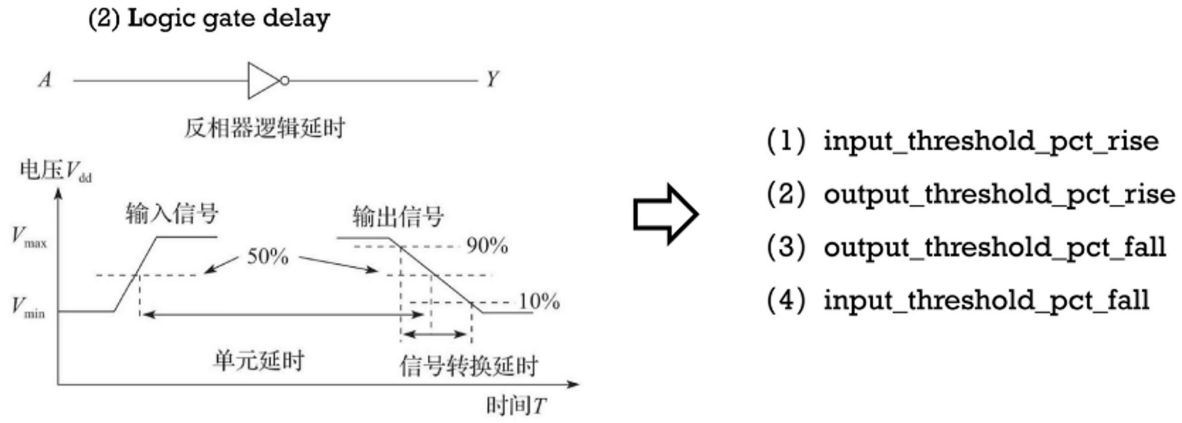


propagation delay

传播延时等于input和output 50%Vdd对应的时间差
受到input transition和output load cap限制：
如果input transition是fast slew，那么cell delay会小
如果输出负载越大，需要给负载充电的时间越长，cell delay越大

1. input_threshold_pct_rise
2. output_threshold_pct_rise

3. output_threshold_pct_fall
4. input_threshold_pct_fall

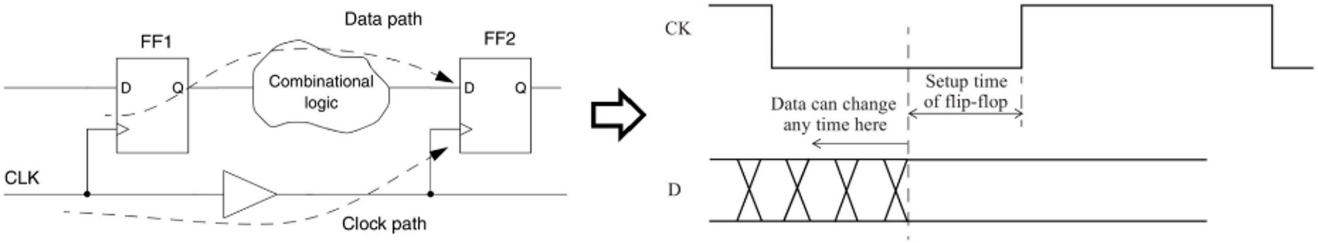


Tf: output fall delay
Tr: output rise delay

setup time
hold time

Setup time and hold time

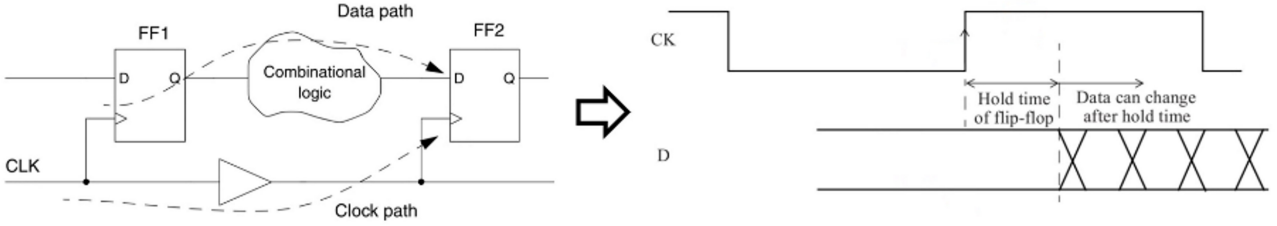
- A setup constraint specifies how much time is necessary for data to be available at the input of a sequential device **before** the clock edge that captures the data in the device.
- This constraint enforces a **maximum** delay on the data path relative to the clock path.



Tc1 + Tco + Tdata < Tc2 + Tclk - Tsetup
0.8s < 2.1s #考虑约束max delay on the data path不要超过2.1s这个setup基准线

Setup time and hold time

- A hold constraint specifies how much time is necessary for data to be stable at the input of a sequential device **after** the clock edge that captures the data in the device.
- This constraint enforces a **minimum** delay on the data path relative to the clock path.



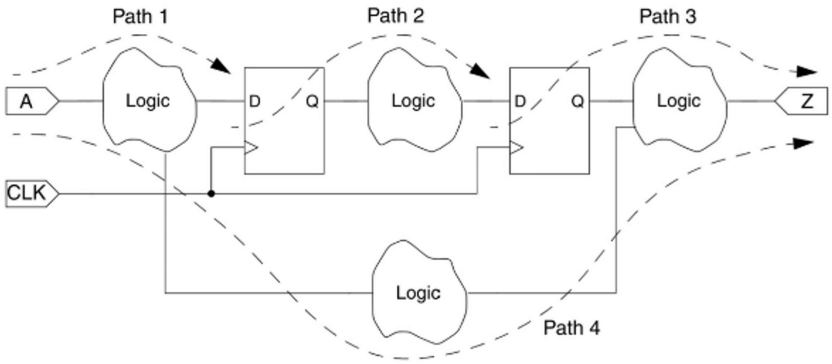
Tc1 + Tco + Tdata > Tc2 + Thold
0.8s > 0.3s #考虑约束min delay on the data path不要低于0.3s的基准线
setup time约束当前信号多久到（max delay）
hold time约束下一个信号多久到（min delay）

静态时序分析会分割整个电路的时序路径，再检查建立时间和保持时间

Timing path

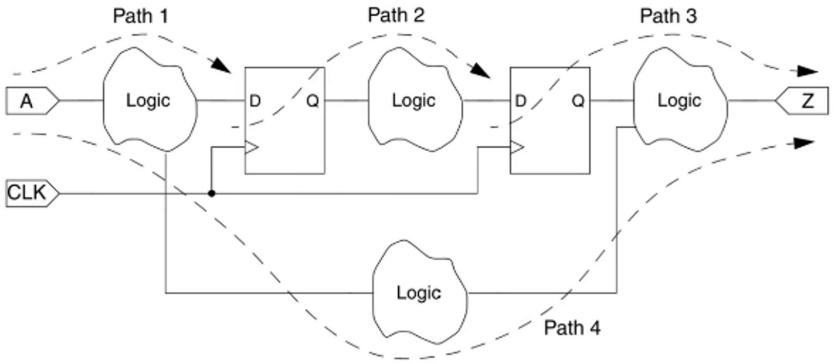
The first step performed by PrimeTime for timing analysis is to break the design down into a set of timing paths.

Each path has **a startpoint** and **an endpoint**.



Timing path

The **startpoint** of a path is a **clock pin** of a sequential element, or possibly an **input port** of the design (because the input data can be launched from some external source).



i. from an input port to an output port,

ii. from an input port to an input of a flip-flop or a memory,

iii. from the clock pin of a flip-flop or a memory to an input of flip-flop or a memory,

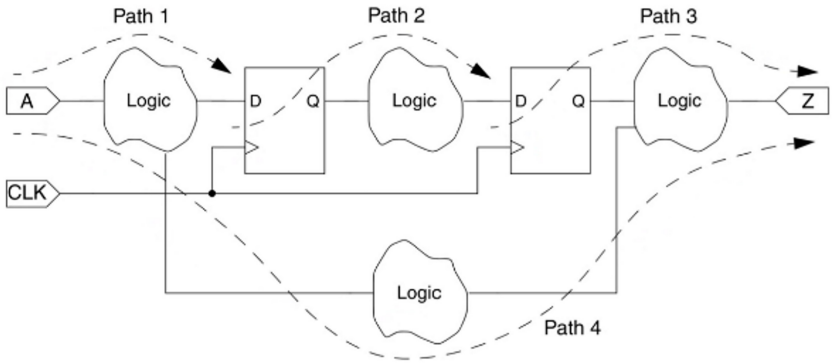
iv. from the clock pin of a flip-flop to an output port,

path的起点定义：

1. D触发器的clock pin（引脚）
2. input port of design # input data来自于external source

Timing path

The **endpoint** of a path is a **data input pin** of a sequential element, or possibly an **output port** of the design (because the output data can be captured by some external sink).



path的终点定义：

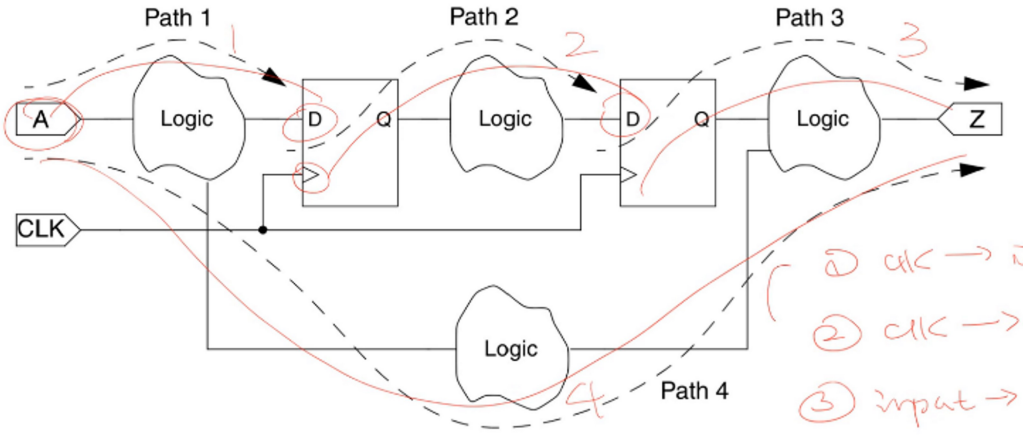
3. D触发器的data input pin
4. output port of design

起点：2
终点：2
path：2 * 2 = 2 4

2-STA Concepts

起点 2
终点 2
2×2=4

Timing path



① clk → D
② clk → output
③ input → D
④ input → output

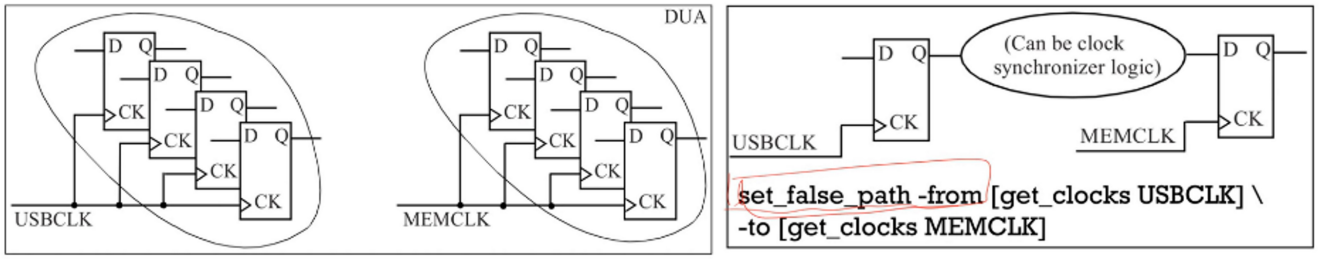
任何电路都可以被这4种典型的path指定

SOC：全局异步，局部同步
时钟域（Clock Domains）：
异步跨时钟域：这些path无法用PT检查，需要加入约束，使PT知道这些path不需要检查它们的setup和hold

2-STA Concepts

Clock Domains

The set of flip-flops being fed by one clock is called its clock domain.



Operating Conditions 操作条件
PVT Process Voltage Temperature
根据特定的PVT计算cell delay和net delay
slow process models, typical process models, fast process models

Operating Conditions

- There are **three** kinds of manufacturing process models that are provided by the semiconductor foundry for digital designs: **slow** process models, **typical** process models, and **fast** process models.
- The slow and fast process models represent the **extreme corners** of the manufacturing process of a foundry.
- For **robust** design, the design is validated at the extreme corners of the manufacturing process as well as environment extremes for temperature and power supply.

extreme corners: 极限条件

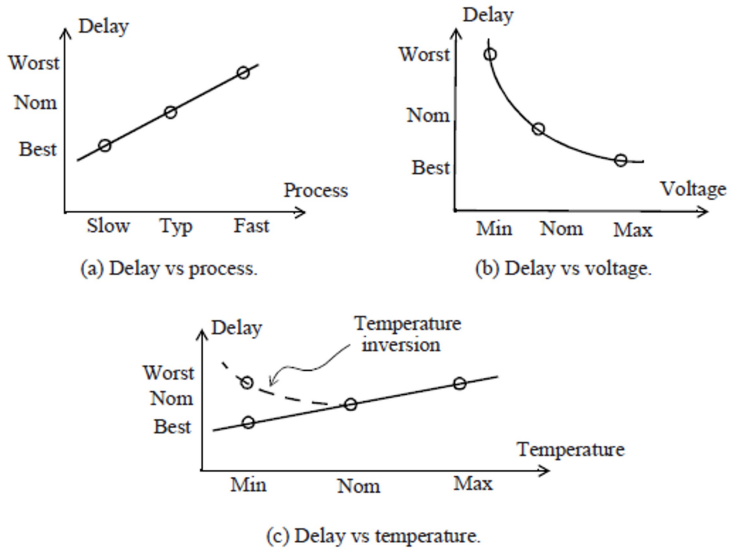


Figure 2-23 *Delay variations with PVT.*

ss (slow slow)(高温低压) >>> max delay >>> setup time
ff (fast fast)(低温高压) >>> min delay >>> hold time

温度和电压根据芯片设计等级（商用级，车规级，航天级）和工艺库限定

2-STA Concepts

Operating Conditions

The choice of what operating condition to use for STA is also governed by the operating conditions under which cell libraries are available. Three standard operating conditions are:

- **WCS (Worst-Case Slow):** Process is slow, temperature is highest (say 125C) and voltage is lowest (say nominal 1.2V minus 10%).
- **TYP (Typical):** Process is typical, temperature is nominal (say 25C) and voltage is nominal (say 1.2V).
- **BCF (Best-Case Fast):** Process is fast, temperature is lowest (say -40C) and voltage is highest (say nominal 1.2V plus 10%).

```
set_operating_conditions "WCCOM" -library mychip
# Use the operating condition called WCCOM defined in the cell library mychip.
```