Time Borrowing

2022年6月10日　　15:19

Time borrowing

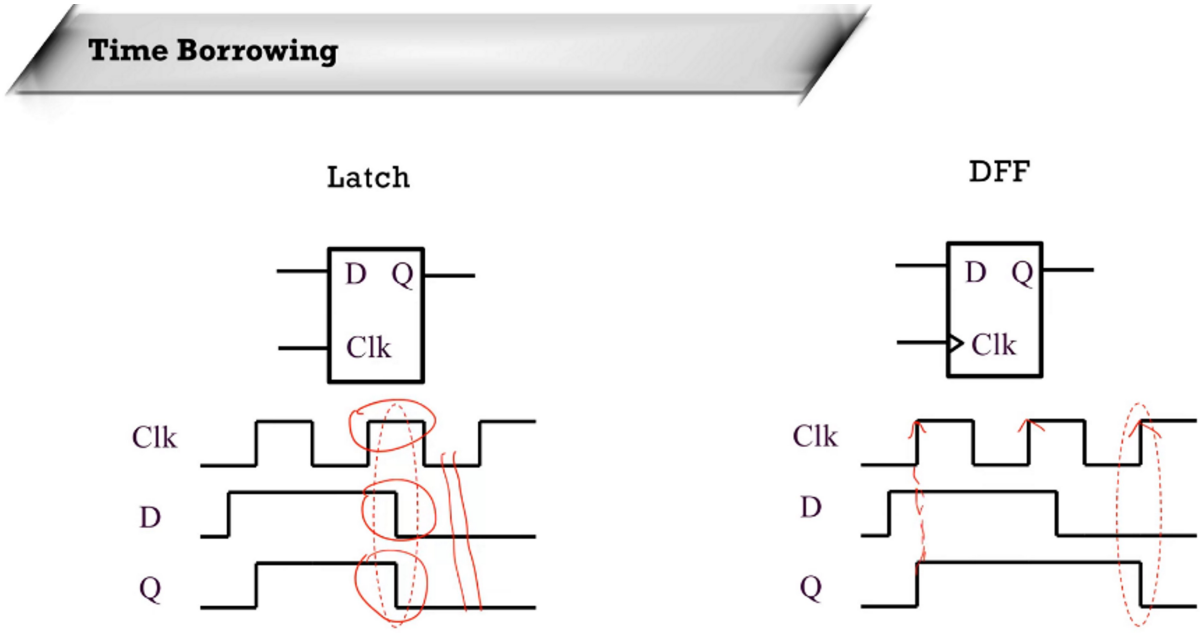
主要针对于latch的电路

latch：

1. 高电平触发，Q=D
2. 低电平触发，保持数据

DFF：

3. 边沿触发
4. Q继承的是在CLK边沿触发，一瞬间D的值，这个值直到下一个CLK边沿才会被刷新

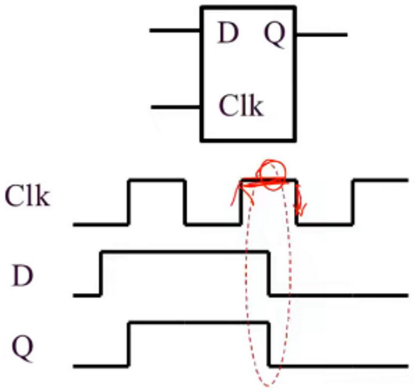


CLK in latch：
opening edge：进入有效电平的沿
closing edge：进入无效电平的沿

Time Borrowing

The time borrowing technique, which is also called cycle stealing, occurs at a latch.

- In a latch, one edge of the clock makes the latch transparent, that is, it opens the latch so that output of the latch is the same as the data input; this clock edge is called the opening edge.
- The second edge of the clock closes the latch, that is, any change on the data input is no longer available at the output of the latch; this clock edge is called the closing edge.



向后面借了时间，使前面的时间大一些

Time Borrowing

Typically, the data should be ready at a latch input before the active edge of the clock. However, since a latch is transparent when the clock is active, the data can arrive later than the active clock edge, that is, it can borrow time from the next cycle.

If such time is borrowed, the time available for the following stage (latch to another sequential cell) is reduced.

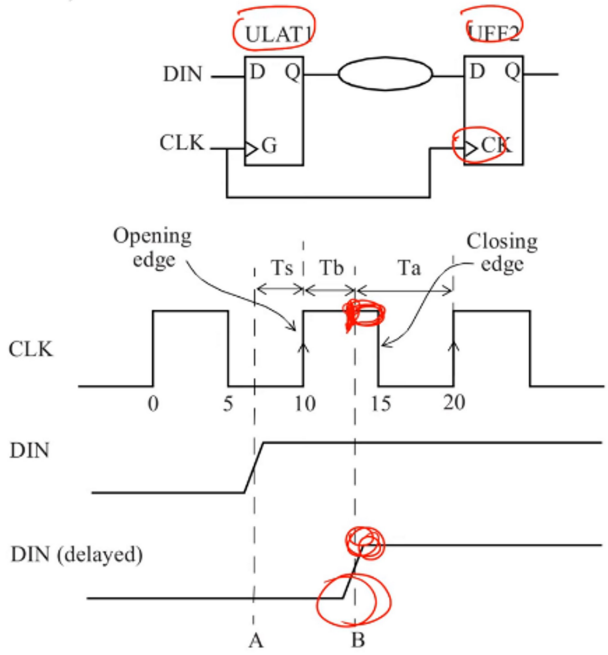
timing borrowing可以给max delay留更多的slack，使setup check更加宽松

Time Borrowing

Here is an example of time borrowing using an active rising edge.

- If data DIN is ready at time A prior to the latch opening on the rising edge of CLK at 10ns, the data flows to the output of the latch as it opens.

If data arrives at time B as shown for DIN (delayed), it borrows time Tb. However, this reduces the time available from the latch to the next flip-flop UFF2 - instead of a complete clock cycle, only time Ta is available.

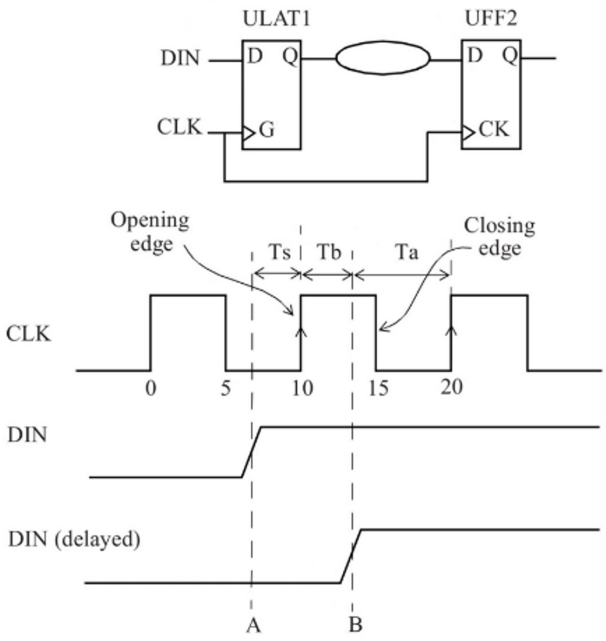


锁存器的时序的第一条规则是：如果数据在锁存器的打开沿之前到达，则寄存器行为将与触发器完全一样。在打开沿捕获数据，而同一时钟沿又将发起数据，作为下一条时序路径的起点。

第二条规则适用的情况是：数据在锁存器为透明状态时（在打开沿和关闭沿之间）到达。锁存器的输出将被用作下一级时序路径的起点，而不是时钟引脚。在锁存器处结束的时序路径所借用的时间将决定下一级的发起时间。

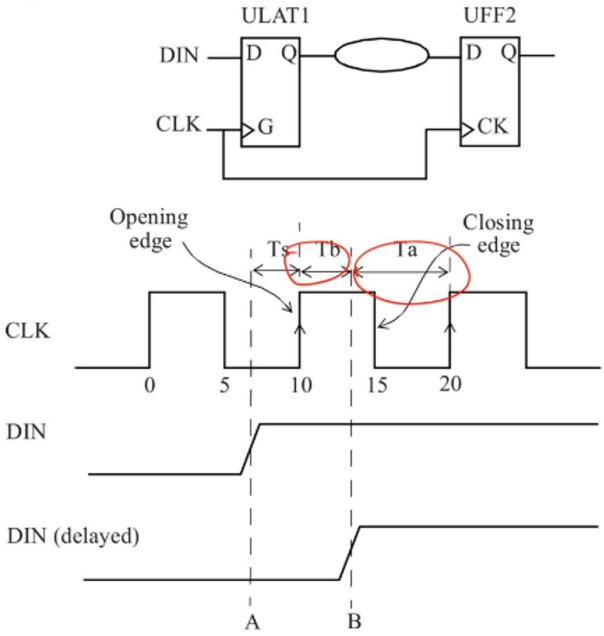
Time Borrowing

- The first rule in timing to a latch is that if the data arrives before the opening edge of the latch, the behavior is modeled exactly like a flip-flop.
- The opening edge captures the data and the same clock edge launches the data as the start point for the next path.



Time Borrowing

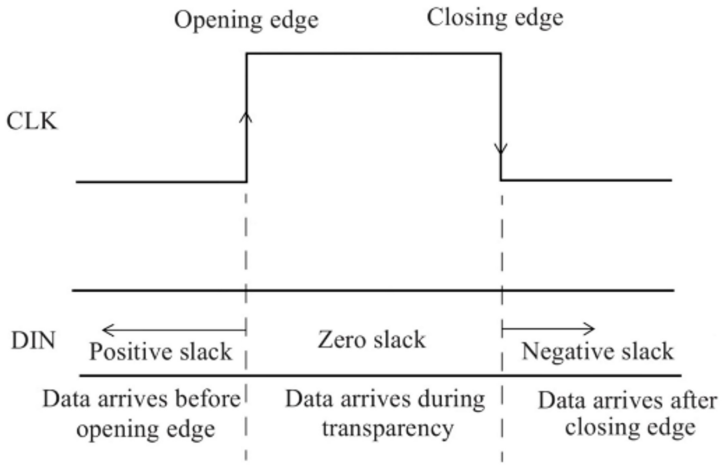
- The second rule applies when the data signal arrives while the latch is transparent (between the opening and the closing edge).
- The output of the latch, rather than the clock pin, is used as the launch point for the next stage.
- The amount of time borrowed by the path ending at the latch determines the launch time for the next stage.



如果在opening edge和closing edge之间数据到来，仍然可以使Q=D，但是closing edge之后数据再到来，就产生violation

Time Borrowing

The timing regions for data arrival for positive slack, zero slack, and negative slack (that is, when a violation occurs).

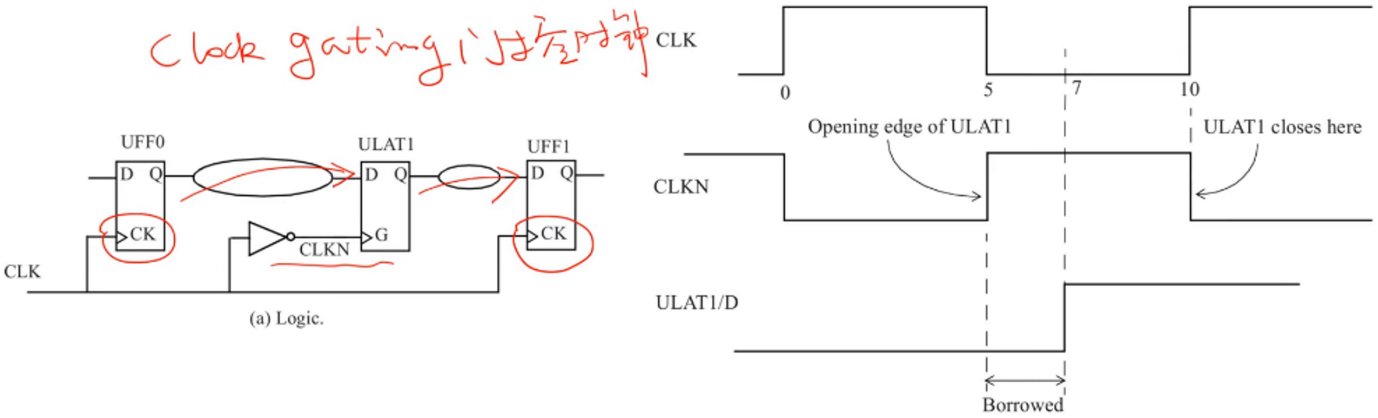


A data signal that arrives after the closing edge at the latch is a timing violation.

Time Borrowing

This is the use of a latch with a half-cycle path to the next stage flip-flop.

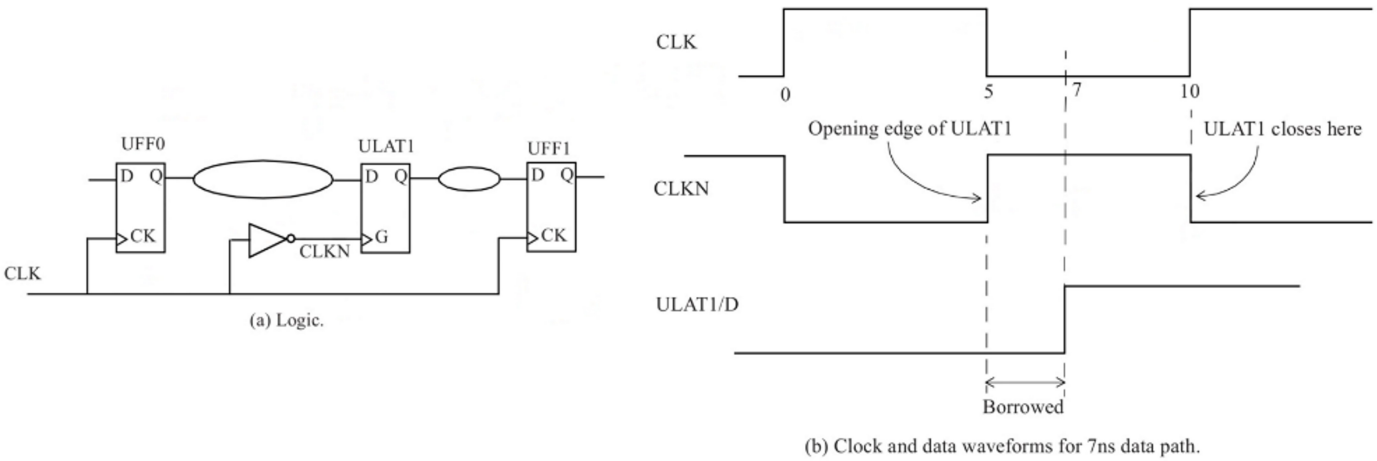
We next describe three sets of timing reports for the latch example of it to illustrate the different amounts of time borrowed from the next stage.



No time borrowing - positive slack

Time Borrowing

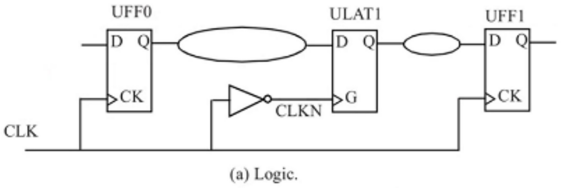
Here is the setup path report when the data path delay from the flip-flop *UFF0* to the latch *ULAT1* is less than 5ns.



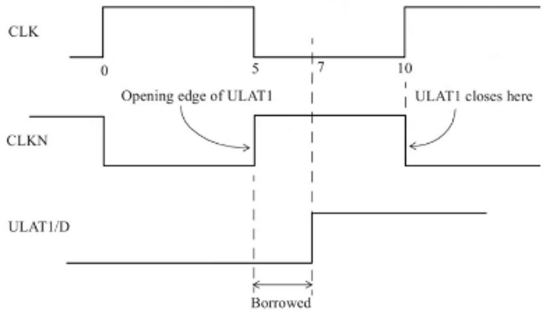
观察时序报告需要查看是否有latch

setup check without time borrowing

Time Borrowing



(a) Logic.

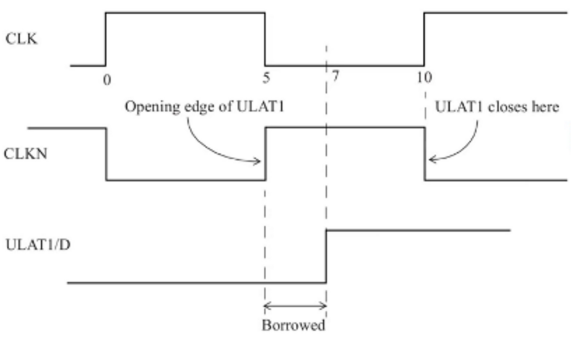


(b) Clock and data waveforms for 7ns data path.

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: ULAT1 (positive level-sensitive latch clocked by CLK')
  Path Group: CLK
  Path Type: max

Point                                              Incr       Path
-----------------------------------------------------------------
clock CLK (rise edge)                              0.00       0.00
clock source latency                               0.00       0.00
clk (in)                                           0.00       0.00 r
UFF0/CK (DF  )                                     0.00       0.00 r
UFF0/Q (DF  )                                      0.12       0.12 r
UBUF0/Z (BUFF  )                                   2.01       2.13 r
UBUF1/Z (BUFF  )                                   2.46       4.59 r
UBUF2/Z (BUFF  )                                   0.07       4.65 r
ULAT1/D (LH  )                                     0.00       4.65 r
data arrival time                                             4.65
```

Time Borrowing



(b) Clock and data waveforms for 7ns data path.

```
clock CLK' (rise edge)                             5.00       5.00
clock source latency                               0.00       5.00
clk (in)                                           0.00       5.00 f
UINV0/ZN (INV  )                                   0.02       5.02 r
ULAT1/G (LH  )                                     0.00       5.02 r
time borrowed from endpoint                        0.00       5.02
data required time                                            5.02
-----------------------------------------------------------------
data required time                                            5.02
data arrival time                                            -4.65
-----------------------------------------------------------------
slack (MET)                                                   0.36

Time Borrowing Information
-------------------------------------------------
CLK' nominal pulse width                   5.00
clock latency difference                  -0.00
library setup time                        -0.01
-------------------------------------------------
max time borrow                            4.99
actual time borrow                         0.00
-------------------------------------------------
```

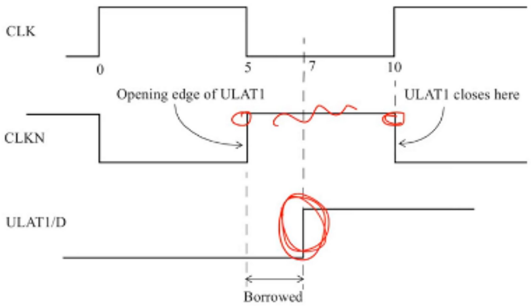
In this case, there is no need to borrow as data reaches the latch ULAT1 in time before the latch opens.

Time brrowing - zero slack

setup check with time borrowing

Time Borrowing

The path report below shows the case where the data path delay from the flip-flop UFF0 to the latch ULAT1 is **greater than 5ns**.



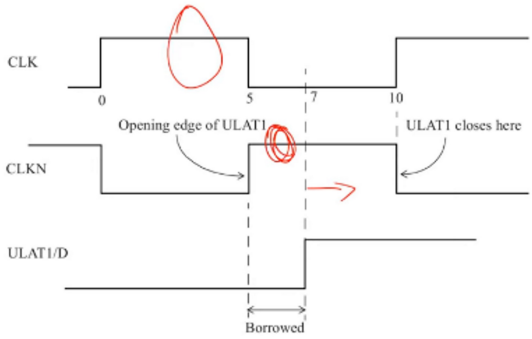
(b) Clock and data waveforms for 7ns data path.

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: ULAT1 (positive level-sensitive latch clocked by CLK')
  Path Group: CLK
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLK (rise edge)                    0.00       0.00
  clock source latency                     0.00       0.00
  clk (in)                                 0.00       0.00 r
  UFF0/CK (DF  )                           0.00       0.00 r
  UFF0/Q (DF  )                            0.12       0.12 r
  UBUF0/Z (BUFF  )                         3.50       3.62 r
  UBUF1/Z (BUFF  )                         3.14       6.76 r
  UBUF2/Z (BUFF  )                         0.07       6.83 r
  ULAT1/D (LH  )                           0.00       6.83 r
  data arrival time                                   6.83
```

在5ns时，新数据还没到来，基于latch在opening edge和closing edge之间的时间点处于透明状态，仍然可以继承数据，所以新数据实际上可以在5ns之后到来，但需要借用下一个周期的时间。此时，计算下一个周期的起点不再是latch CLK的pin，而是latch Q的pin

Time Borrowing



(b) Clock and data waveforms for 7ns data path.

```
  clock CLK' (rise edge)                   5.00       5.00
  clock source latency                     0.00       5.00
  clk (in)                                 0.00       5.00 f
  UINV0/ZN (INV  )                         0.02       5.02 r
  ULAT1/G (LH  )                           0.00       5.02 r
  time borrowed from endpoint              1.81       6.83
  data required time                                  6.83
  -----------------------------------------------------------
  data required time                                  6.83
  data arrival time                                  -6.83
  -----------------------------------------------------------
  slack (MET)                                         0.00

  Time Borrowing Information
  -------------------------------------------------
  CLK' nominal pulse width                 5.00
  clock latency difference                -0.00
  library setup time                      -0.01
  -------------------------------------------------
```

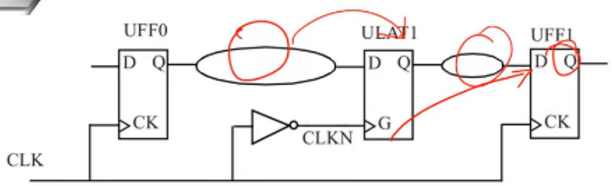
In this case, since the data becomes available while the latch is transparent, the required delay of 1.81ns is borrowed from the subsequent path and the timing is still met.

借用的时间会加在后面的路径

setup check on the latter path with time borrowing

Time Borrowing

Here is the path report of the subsequent path showing that 1.81ns was already borrowed by the previous path.



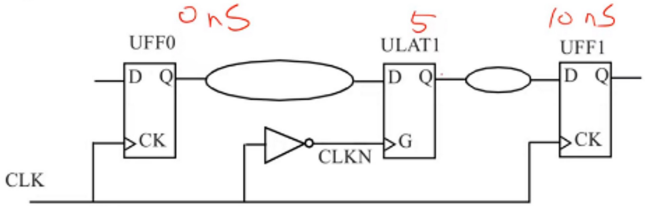
(a) Logic.

```
Startpoint: ULAT1 (positive level-sensitive latch clocked by CLK')
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Point                                          Incr       Path
  -----------------------------------------------------------------
  clock CLK' (rise edge)                         5.00       5.00
  clock source latency                           0.00       5.00
  clk (in)                                       0.00       5.00 f
  UINV0/ZN (INV  )                               0.02       5.02 r
  ULAT1/G (LH  )                                 0.00       5.02 r
  time given to startpoint                       1.81       6.83
  ULAT1/QN (LH  )                                0.13       6.95 f
  UFF1/D (DF  )                                  0.00       6.95 f
  data arrival time                                         6.95
```

Time Borrowing

Here is the path report of the subsequent path showing that 1.81ns was already borrowed by the previous path.



(a) Logic.

```
  clock CLK (rise edge)                          10.00      10.00
  clock source latency                            0.00      10.00
  clk (in)                                        0.00      10.00 r
  UFF1/CK (DF  )                                  0.00      10.00 r
  library setup time                             -0.04       9.96
  data required time                                         9.96
  -----------------------------------------------------------------
  data required time                                         9.96
  data arrival time                                         -6.95
  -----------------------------------------------------------------
  slack (MET)                                                3.01
```

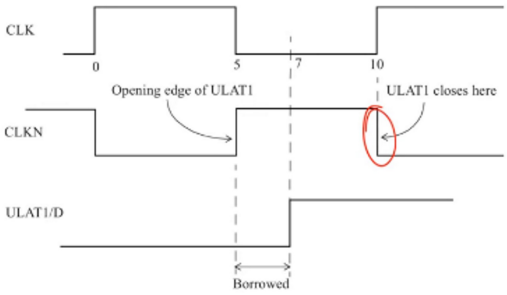
Timing brrowing - negative slack

setup check with time borrowing but creates nagative slack

Time Borrowing

In this case, the data path delay is much larger and data becomes available only after the latch closes.

This is clearly a timing violation.



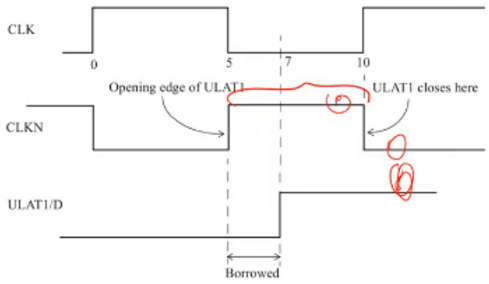
(b) Clock and data waveforms for 7ns data path.

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: ULAT1 (positive level-sensitive latch clocked by CLK')
  Path Group: CLK
  Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CLK (rise edge)                    0.00       0.00
clock source latency                     0.00       0.00
clk (in)                                 0.00       0.00 r
UFF0/CK (DF  )                           0.00       0.00 r
UFF0/Q (DF  )                            0.12       0.12 r
UBUF0/Z (BUFF  )                         6.65       6.77 r
UBUF1/Z (BUFF  )                         4.33      11.10 r
UBUF2/Z (BUFF  )                         0.07      11.17 r
ULAT1/D (LH  )                           0.00      11.17 r
data arrival time                                  11.17
```

Time Borrowing

In this case, the data path delay is much larger and data becomes available only after the latch closes. This is clearly a timing violation.



(b) Clock and data waveforms for 7ns data path.

```
clock CLK' (rise edge)                   5.00       5.00
clock source latency                     0.00       5.00
clk (in)                                 0.00       5.00 f
UINV0/ZN (INV  )                         0.02       5.02 r
ULAT1/G (LH  )                           0.00       5.02 r
time borrowed from endpoint             -4.99      10.00
data required time                                 10.00
-----------------------------------------------------------
data required time                                 10.00
data arrival time                                 -11.17
-----------------------------------------------------------
slack (VIOLATED)                                   -1.16

Time Borrowing Information
-------------------------------------------------
CLK' nominal pulse width                 5.00
clock latency difference                -0.00
library setup time                      -0.01
-------------------------------------------------
max time borrow                          4.99
actual time borrow                       4.99
-------------------------------------------------
```