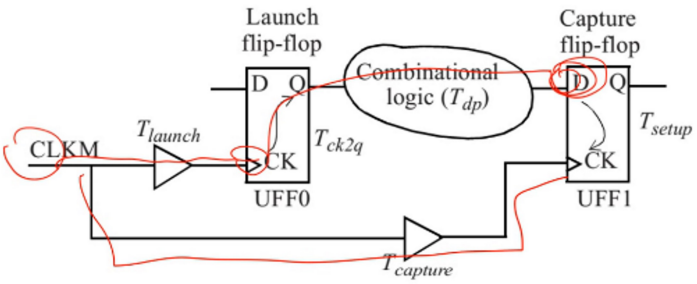
Setup check && Hold check

2022年6月9日　　14:13

Setup timing check

1. 记住end point check
2. 记住end point对应的clock才属于path group
3. path_type: max = setup check
4. path_type: min = hold check

Setup Timing Check



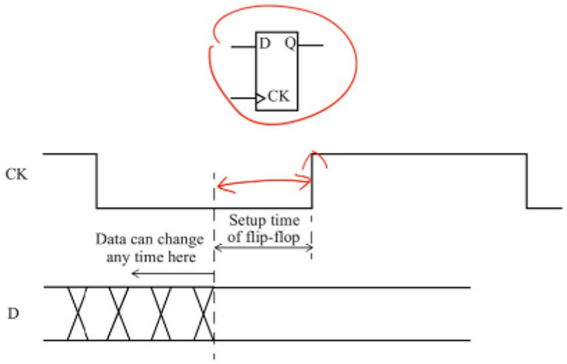
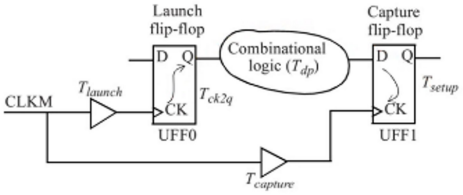
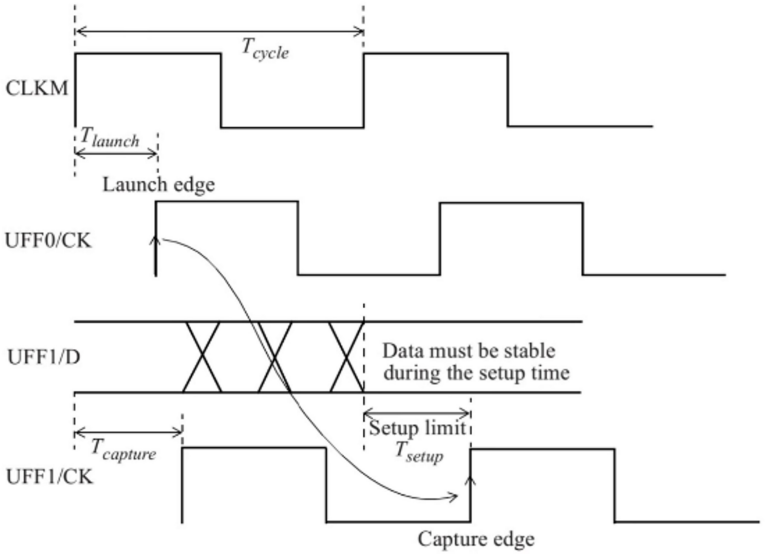


Figure 8-1 *Setup requirement of a flip-flop.*

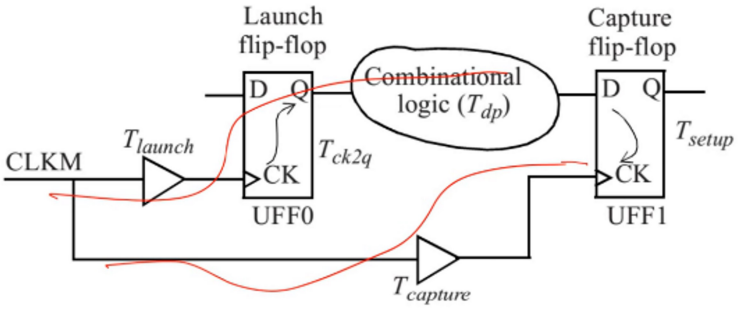
2+2=4

Setup Timing Check





Setup Timing Check



The setup check can be mathematically expressed as:

$$T_{launch} + T_{ck2q} + T_{dp} < T_{capture} + T_{cycle} - T_{setup}$$

path type: max(max delay)(slow)
max delay = Tlaunch + Tck2q + Tdp
path group: clkm(check endpoint)
r && f表示rising && falling
Tarrive

Setup Timing Check

1、Flip-flop to Flip-flop Path

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                          Incr       Path
-----------------------------------------------------------------
clock CLKM (rise edge)                         0.00       0.00
clock network delay (ideal)                    0.00       0.00
UFF0/CK (DFF )                                 0.00       0.00 r
UFF0/Q (DFF ) <-                               0.16       0.16 f
UNOR0/ZN (NR2  )                               0.04       0.20 r
UBUF4/Z (BUFF  )                               0.05       0.26 r
UFF1/D (DFF )                                  0.00       0.26 r
data arrival time                                         0.26
```

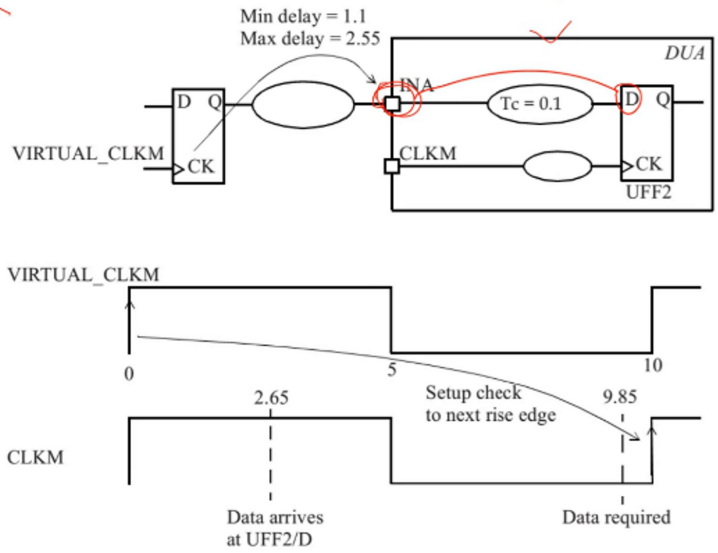
uncertainty >>> clock skew and jitter >>> for more pessimism
Tarrive <= Trequired
slack = Tarrive - Trequired >=0

1、Flip-flop to Flip-flop Path

```
clock CLKM (rise edge)                          10.00      10.00
clock network delay (ideal)                      0.00      10.00
clock uncertainty                               -0.30       9.70
UFF1/CK (DFF )                                              9.70 r
library setup time                              -0.04       9.66
data required time                                          9.66
-----------------------------------------------------------------
data required time                                          9.66
data arrival time                                          -0.26
-----------------------------------------------------------------
slack (MET)                                                 9.41
```

Setup Timing Check

2、Input to Flip-flop Path



1. 虚拟时钟作为真实时钟的参考基准
2. set_input_delay基于虚拟时钟

Timing Analysis——Setup Timing Check

Constrain:

creat_clock –name VIRTUAL_CLKM –period 10 –waveform {0 5}

set_input_delay –clock VIRTUAL_CLKM –max 2.55 [get_ports INA]

对于input port和output port分别需要加入set_driving_cell和set_load

input_delay是考虑了setup time能满足的情况下，input port到D pin的delay time是否可以有slack，是否可以使Tarrive < Trequired

setup check if input delays exist

8.1.2 Input to Flip-flop Path

Here is an example path report through an input port to a flip-flop. Figure 8-4 shows the schematic related to the input path and the clock waveforms.

```
Startpoint: INA (input port clocked by VIRTUAL_CLKM)
Endpoint: UFF2 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock VIRTUAL_CLKM (rise edge)           0.00       0.00
clock network delay (ideal)              0.00       0.00
input external delay                     2.55       2.55 f
```

```
INA (in) <-                                0.00       2.55 f
UINV1/ZN (INV  )                           0.02       2.58 r
UAND0/Z (AN2  )                            0.06       2.63 r
UINV2/ZN (INV  )                           0.02       2.65 f
UFF2/D (DFF )                              0.00       2.65 f
data arrival time                                     2.65

clock CLKM (rise edge)                    10.00      10.00
clock source latency                       0.00      10.00
CLKM (in)                                  0.00      10.00 r
UCKBUF0/C (CKB  )                          0.06      10.06 r
UCKBUF2/C (CKB  )                          0.07      10.12 r
UCKBUF3/C (CKB  )                          0.06      10.18 r
UFF2/CK (DFF )                             0.00      10.18 r
clock uncertainty                         -0.30       9.88
library setup time                        -0.03       9.85
data required time                                    9.85
-----------------------------------------------------------
data required time                                    9.85
data arrival time                                    -2.65
-----------------------------------------------------------
slack (MET)                                           7.20
```

The first thing to notice is *input port clocked by VIRTUAL_CLKM*. As discussed in Section 7.9, this clock can be considered as an imaginary (virtual) flip-flop outside of the design that is driving the input port *INA* of the design. The clock of this virtual flip-flop is *VIRTUAL_CLKM*. In addition, the max delay from the clock pin of this virtual flip-flop to the input port *INA* is specified as 2.55ns - this appears as *input external delay* in the report. Both of these parameters are specified using the following SDC commands.

```
create_clock -name VIRTUAL_CLKM -period 10 -waveform {0 5}
set_input_delay -clock VIRTUAL_CLKM \
  -max 2.55 [get_ports INA]
```

Notice that the definition of the virtual clock *VIRTUAL_CLKM* does not have any pin from the design associated with it; this is because it is considered to be defined outside of the design (it is *virtual*). The input delay spec-

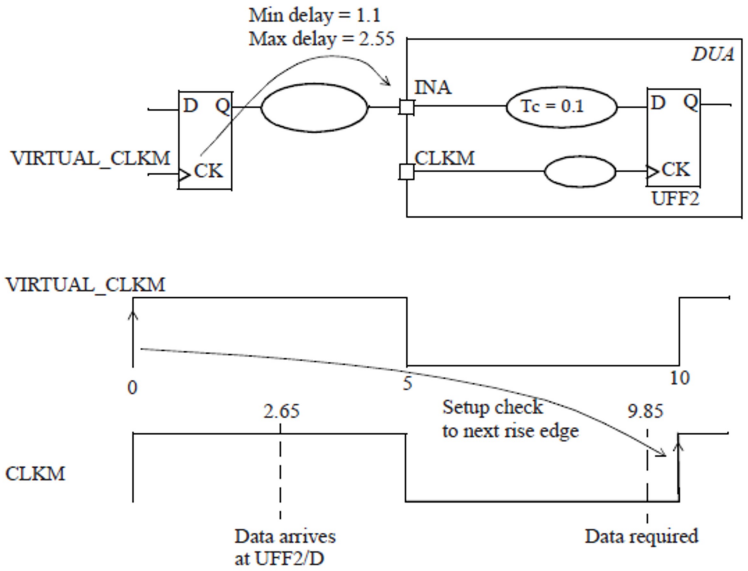


Figure 8-4 *Setup check for the path through input port.*

ification, *set_input_delay*, specifies the delay with respect to the virtual clock.

The input path starts from the port *INA*; how does one compute the delay of the first cell *UINV1* connected to port *INA*? One way to accomplish this is by specifying the driving cell of the input port *INA*. This driving cell is used to determine the drive strength and thus the slew on the port *INA*, which is then used to compute the delay of the cell *UINV1*. In the absence of any slew specification on the input port *INA*, the transition at the port is assumed to be ideal, which corresponds to a transition time of 0ns.

```
set_driving_cell -lib_cell BUFF \
  -library lib013lwc [get_ports INA]
```

Figure 8-4 also shows how the setup check is done. The time by which data must arrive at *UFF2/D* is 9.85ns. However, the data arrives at 2.65ns, thus the report shows a positive slack of 7.2ns on this path.

Flip-flop to Output Path

Setup Timing Check

3、Flip-flop to Output Path

Similar to the input port constraint described above, an output port can be constrained either with respect to a virtual clock, or an internal clock of the design, or an input clock port, or an output clock port.

To determine the delay of the last cell connected to the output port correctly, **one needs to specify the load on this port**. The output load is specified above using the **set_load** command.

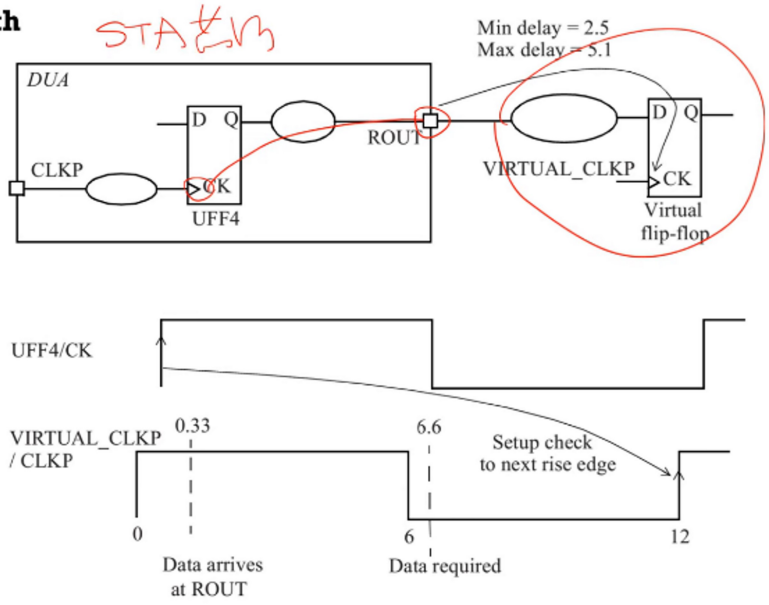
Setup Timing Check

3、Flip-flop to Output Path

```
set_output_delay -clock VIRTUAL_CLKP \
  -max 5.1 [get_ports ROUT]
set_load 0.02 [get_ports ROUT]
```

Setup Timing Check

3、Flip-flop to Output Path



Setup Timing Check

3、Flip-flop to Output Path

```
Startpoint: UFF4 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: ROUT (output port clocked by VIRTUAL_CLKP)
  Path Group: VIRTUAL_CLKP
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKP (in)                                          0.00       0.00 r
  UCKBUF4/C (CKB  )                                  0.06       0.06 r
  UCKBUF5/C (CKB  )                                  0.06       0.12 r
  UFF4/CK (DFF )                                     0.00       0.12 r
  UFF4/Q (DFF )                                      0.13       0.25 r
  UBUF3/Z (BUFF  )                                   0.09       0.33 r
  ROUT (out)                                         0.00       0.33 r
  data arrival time                                             0.33
```

Setup Timing Check

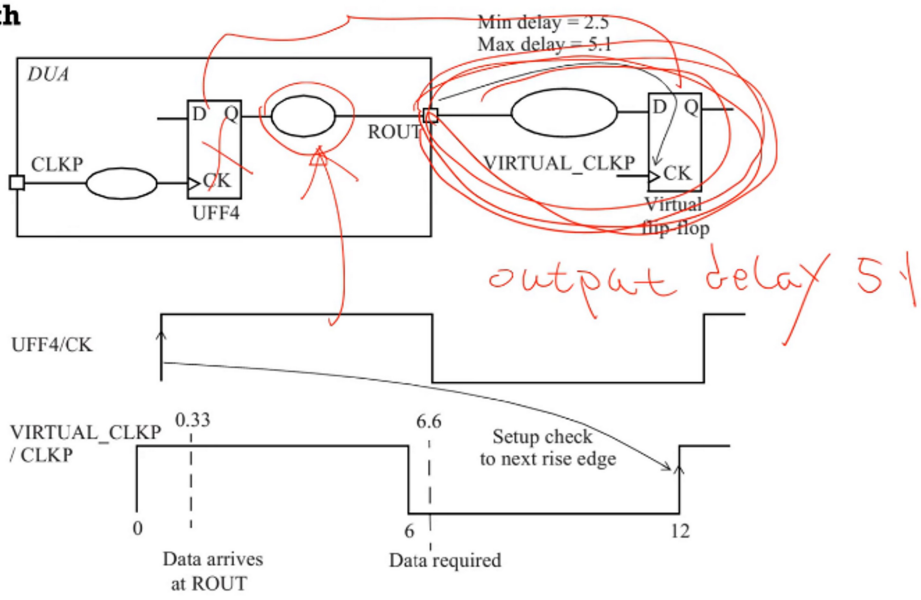
3、Flip-flop to Output Path

```
clock VIRTUAL_CLKP (rise edge)          12.00       12.00
clock network delay (ideal)              0.00       12.00
clock uncertainty                       -0.30       11.70
output external delay                   -5.10        6.60
-------------------------------------------------------------
data required time                                   6.60
data arrival time                                   -0.33
-------------------------------------------------------------
slack (MET)                                          6.27
```

the value of output_delay: 5.1 has included the setup time
output_delay是考虑了setup time能满足的情况下，clock pin到output port的delay time
是否可以有slack，是否可以使Tarrive < Trequired

Setup Timing Check

3、Flip-flop to Output Path



setup check if output delays exist

8.1.3 Flip-flop to Output Path

Similar to the input port constraint described above, an output port can be constrained either with respect to a virtual clock, or an internal clock of the design, or an input clock port, or an output clock port. Here is an example that shows the output pin *ROUT* constrained with respect to a virtual clock. The output constraint is as follows:

```
set_output_delay -clock VIRTUAL_CLKP \
  -max 5.1 [get_ports ROUT]
set_load 0.02 [get_ports ROUT]
```

To determine the delay of the last cell connected to the output port correctly, one needs to specify the load on this port. The output load is specified above using the *set_load* command. Note that the port *ROUT* may have load contribution internal to the *DUA* and the *set_load* specification provides the additional load, which is the load contribution from outside the DUA. In the absence of the *set_load* specification, a value of 0 for the external load is assumed (which may not be realistic as this design would most probably be used in some other design). Figure 8-6 shows the timing path to the virtual flip-flop that has the virtual clock.

The path report through the output port is shown next.

```
Startpoint: UFF4 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: ROUT (output port clocked by VIRTUAL_CLKP)
  Path Group: VIRTUAL_CLKP
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLKP (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  CLKP (in)                                0.00       0.00 r
```

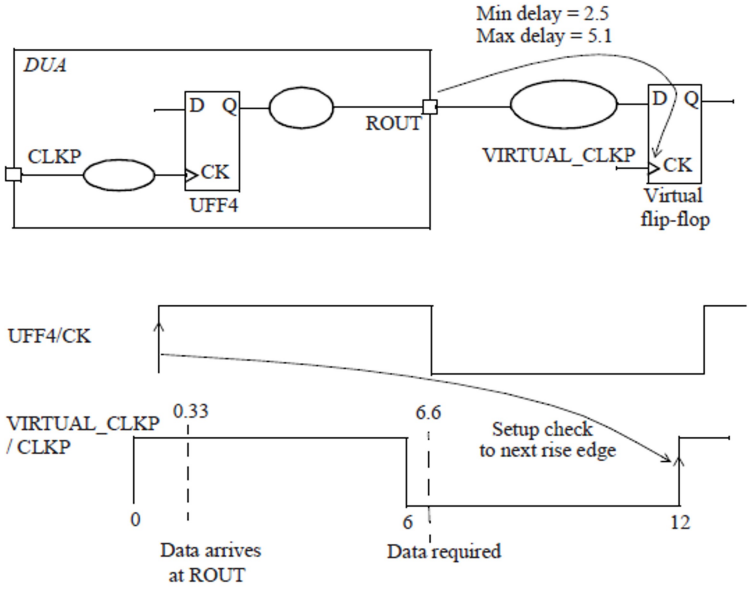


Figure 8-6 *Setup check for path through output port.*

```
  UCKBUF4/C (CKB  )                        0.06       0.06 r
  UCKBUF5/C (CKB  )                        0.06       0.12 r
  UFF4/CK (DFF )                           0.00       0.12 r
  UFF4/Q (DFF )                            0.13       0.25 r
  UBUF3/Z (BUFF  )                         0.09       0.33 r
  ROUT (out)                               0.00       0.33 r
  data arrival time                                   0.33

  clock VIRTUAL_CLKP (rise edge)          12.00      12.00
  clock network delay (ideal)              0.00      12.00
  clock uncertainty                       -0.30      11.70
  output external delay                   -5.10       6.60
  data required time                                  6.60
```

```
------------------------------------------------------------
data required time                                    6.60
data arrival time                                    -0.33
------------------------------------------------------------
slack (MET)                                           6.27
```

Notice that the output delay specified appears as *output external delay* and behaves like a required setup time for the virtual flip-flop.

同时考虑input_delay和output_delay，即delay包括了当前和下一个的setup time，取max delay的情况，那么中间的logic是否能满足max delay下仍然有slack，使Tarrive < Trequired，这样才能满足前后的setup time

Setup Timing Check

4、Input to Output Path

Here are the input and output delay specifications.

```
set_input_delay -clock VIRTUAL_CLKM \
  -max 3.6 [get_ports INB]
set_output_delay -clock VIRTUAL_CLKM \
  -max 5.8 [get_ports POUT]
```

setup check if both input delays and output delays exist

Setup Timing Check

4、Input to Output Path

```
Startpoint: INB (input port clocked by VIRTUAL_CLKM)
Endpoint: POUT (output port clocked by VIRTUAL_CLKM)
Path Group: VIRTUAL_CLKM
Path Type: max

Point                                          Incr       Path
-------------------------------------------------------------
clock VIRTUAL_CLKM (rise edge)                 0.00       0.00
clock network delay (ideal)                    0.00       0.00
```

Setup Timing Check

4、Input to Output Path

input external delay	**3.60**	3.60 f
INB (in) <-	0.00	3.60 f
UBUF0/Z (BUFF)	0.05	3.65 f
UBUF1/Z (BUFF)	0.06	3.72 f
UINV3/ZN (INV)	0.34	4.06 r
POUT (out)	0.00	4.06 r
data arrival time		4.06
clock VIRTUAL_CLKM (rise edge)	10.00	10.00
clock network delay (ideal)	0.00	10.00

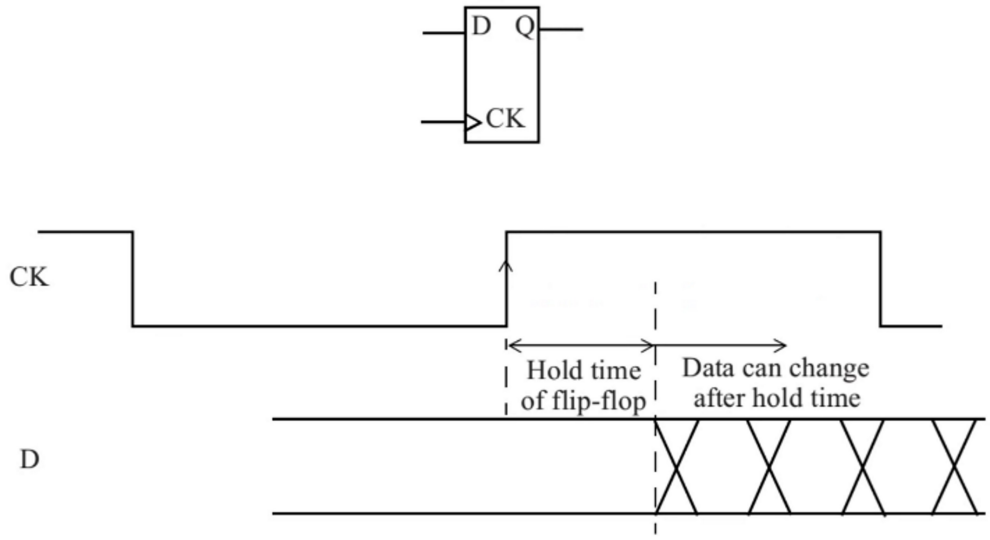
Setup Timing Check

4、Input to Output Path

clock uncertainty	-0.30	9.70
output external delay	**-5.80**	3.90
data required time		3.90
---	---	---
data required time		3.90
data arrival time		-4.06
---	---	---
slack (VIOLATED)		-0.16

Hold time check

Hold Timing Check



Hold Timing Check

Just like the setup check, a hold timing check is between the launch flipflop - the flip-flop that launches the data, and the capture flip-flop - the flip-flop that captures the data and whose hold time must be satisfied.

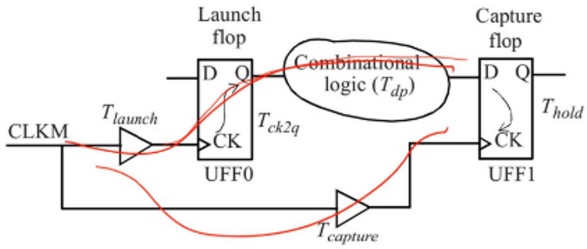
The clocks to these two flip-flops can be the same or can be different.

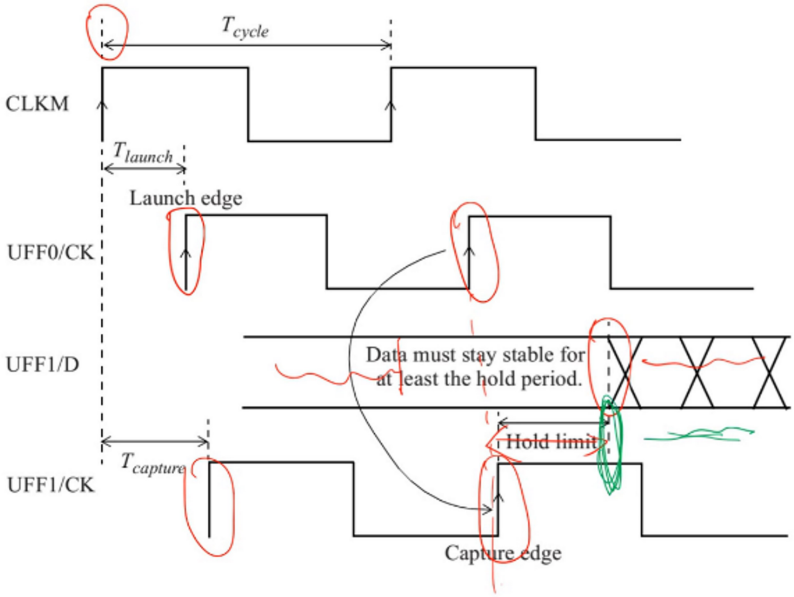
对于单个周期延迟计算，hold check与时钟周期无关，hold check在setup check的前一个周期

Hold Timing Check

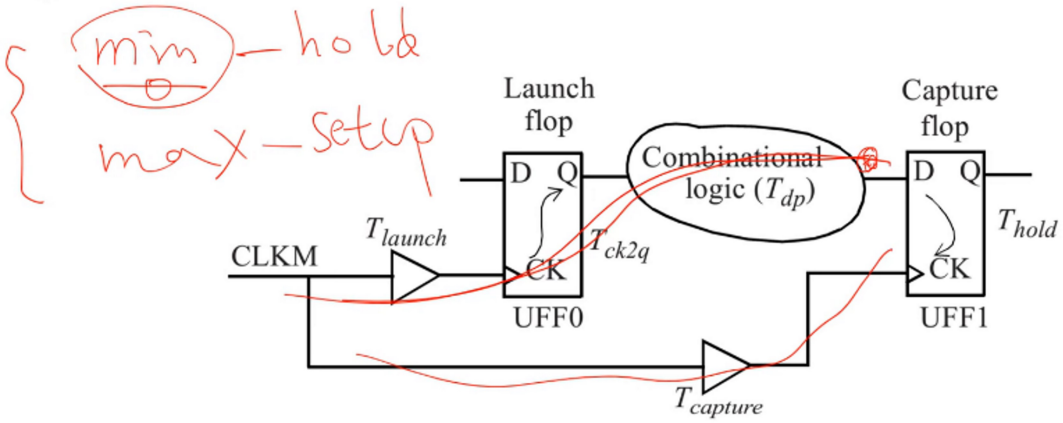
- The hold check is from one active edge of the clock in the launch flip-flop to **the same clock edge** at the capture flip-flop.
- Thus, a hold check is **independent** of the clock period.
- The hold check is carried out on each active edge of the clock of the capture flip-flop.

Hold Timing Check





Hold Timing Check



The hold check can be mathematically expressed as:

$$T_{launch} + T_{ck2q} + T_{dp} > T_{capture} + T_{hold}$$

hold check for reg2reg

Hold Timing Check

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKM (in)                                          0.00       0.00 r
  UCKBUF0/C (CKB  )                                  0.06       0.06 r
  UCKBUF1/C (CKB  )                                  0.06       0.11 r
  UFF0/CK (DFF )                                     0.00       0.11 r
  UFF0/Q (DFF ) <-                                   0.14       0.26 r
  UNOR0/ZN (NR2  )                                   0.02       0.28 f
  UBUF4/Z (BUFF  )                                   0.06       0.33 f
  UFF1/D (DFF )                                      0.00       0.33 f
  data arrival time                                             0.33

  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
```

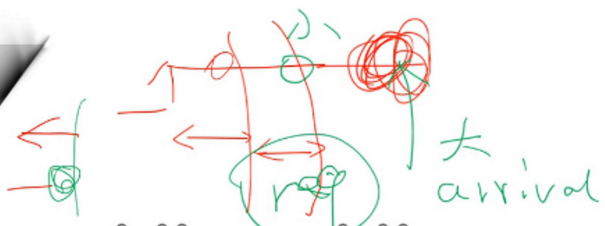
clock uncertainty变得严苛是需要在hold check为正值

Hold Timing Check

CLKM (in)	0.00	0.00 r
UCKBUF0/C (CKB)	0.06	0.06 r
UCKBUF2/C (CKB)	0.07	0.12 r
UFF1/CK (DFF)	0.00	0.12 r
clock uncertainty	0.05	0.17
library hold time	**0.01**	0.19
data required time		0.19
data required time		0.19
data arrival time		-0.33
slack (MET)		0.14

For hold time check, Trequired < Tarrive

Hold Timing Check



CLKM (in)	0.00	0.00 r
UCKBUF0/C (CKB)	0.06	0.06 r
UCKBUF2/C (CKB)	0.07	0.12 r
UFF1/CK (DFF)	0.00	0.12 r
clock uncertainty	+ 0.05	0.17
library hold time	**0.01**	0.19
data required time		0.19
data required time		0.19
data arrival time		-0.33
slack (MET)		0.14

Hold Timing Check

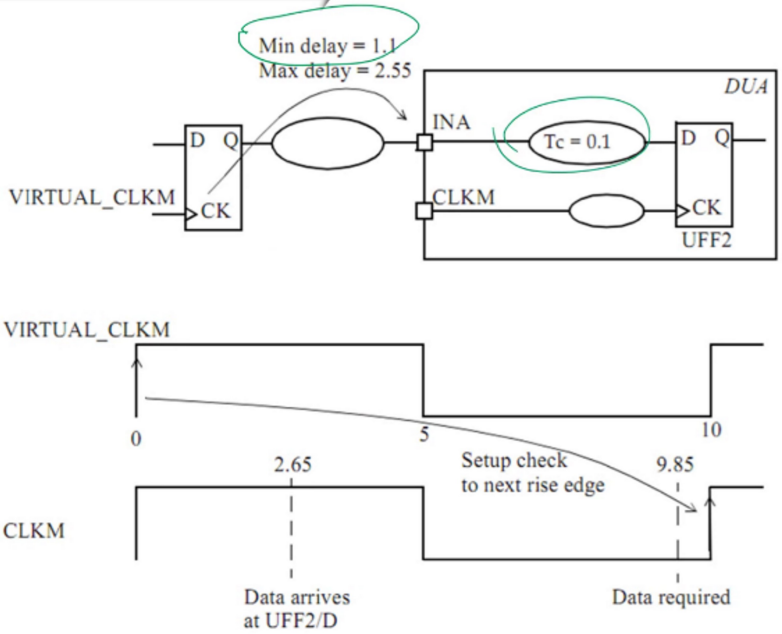
Hold Slack Calculation:

- An interesting point to note is the difference in the way the slack is computed for setup and hold timing reports.
- In the setup timing reports, the arrival time and the required time are computed and the slack is computed to be the required time minus arrival time.

Input port to D pin

Hold Timing Check

1、Input to Flip-flop Path




```
set_input_delay -clock VIRTUAL_CLKM \ -min 1.1 [get_ports INA]
```

hold check if input delays exist

Hold Timing Check

Path Group: CLKM
Path Type: **min**

Point	Incr	Path	
clock VIRTUAL_CLKM (rise edge)	**0.00**	0.00	
clock network delay (ideal)	0.00	0.00	
input external delay	**1.10**	1.10	f
INA (in) <-	0.00	1.10	f
UINV1/ZN (INV)	0.02	1.13	r
UAND0/Z (AN2)	0.06	1.18	r
UINV2/ZN (INV)	0.02	1.20	f
UFF2/D (DFF)	0.00	1.20	f
data arrival time		1.20	

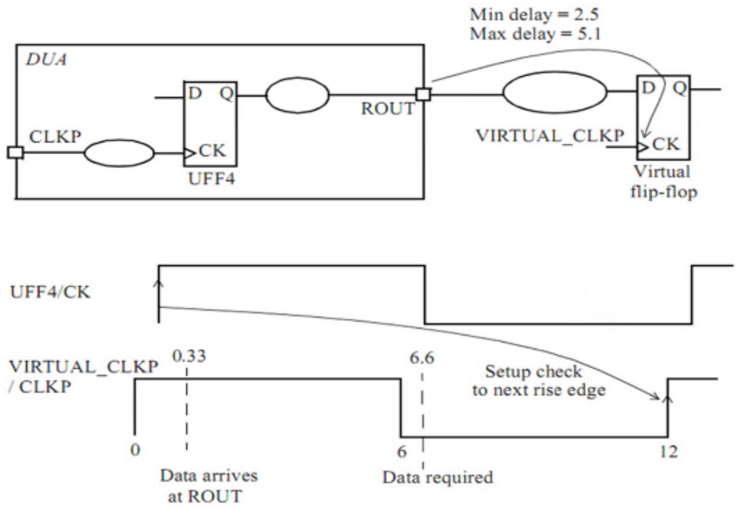
Hold Timing Check

clock CLKM (rise edge)	**0.00**	0.00	
clock source latency	0.00	0.00	
CLKM (in)	0.00	0.00	r
UCKBUF0/C (CKB)	0.06	0.06	r
UCKBUF2/C (CKB)	0.07	0.12	r
UCKBUF3/C (CKB)	0.06	0.18	r
UFF2/CK (DFF)	0.00	0.18	r
clock uncertainty	0.05	0.23	
library hold time	0.01	0.25	
data required time		0.25	
data required time		**0.25**	
data arrival time		**-1.20**	
slack (MET)		**0.95**	

Clock pin to output port

Hold Timing Check

2、Flip-flop to Output Path



set_output_delay -clock VIRTUAL_CLKP \ -min 2.5 [get_ports ROUT]

hold check if output delays exist

Hold Timing Check

2、Flip-flop to Output Path

```
Startpoint: UFF4 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: ROUT (output port clocked by VIRTUAL_CLKP)
  Path Group: VIRTUAL_CLKP
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLKP (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  CLKP (in)                                0.00       0.00 r
  UCKBUF4/C (CKB  )                        0.06       0.06 r
  UCKBUF5/C (CKB  )                        0.06       0.12 r
  UFF4/CK (DFF )                           0.00       0.12 r
  UFF4/Q (DFF )                            0.13       0.25 f
  UBUF3/Z (BUFF  )                         0.08       0.33 f
  ROUT (out)                               0.00       0.33 f
  data arrival time                                   0.33
```

Hold Timing Check

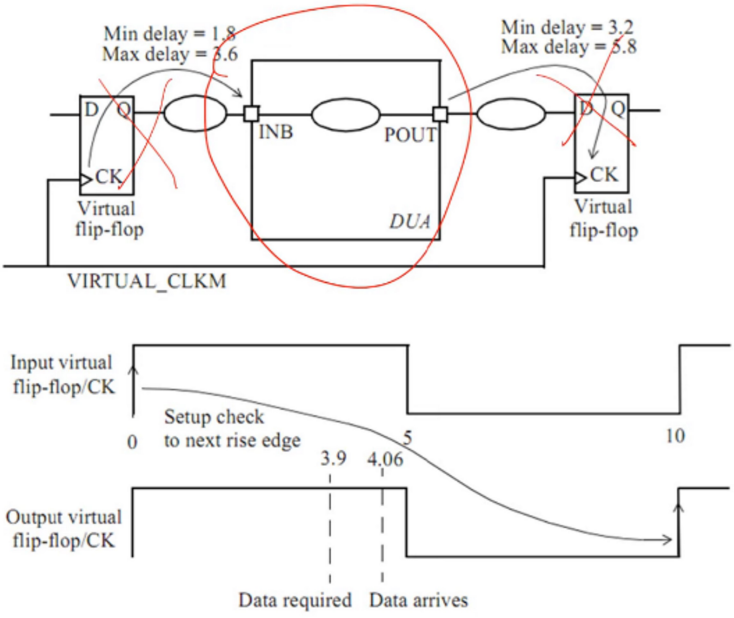
2、Flip-flop to Output Path

clock VIRTUAL_CLKP (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
clock uncertainty	0.05	0.05
output external delay	**-2.50**	-2.45
data required time		-2.45
data required time		-2.45
data arrival time		-0.33
slack (MET)		2.78

input port to output port

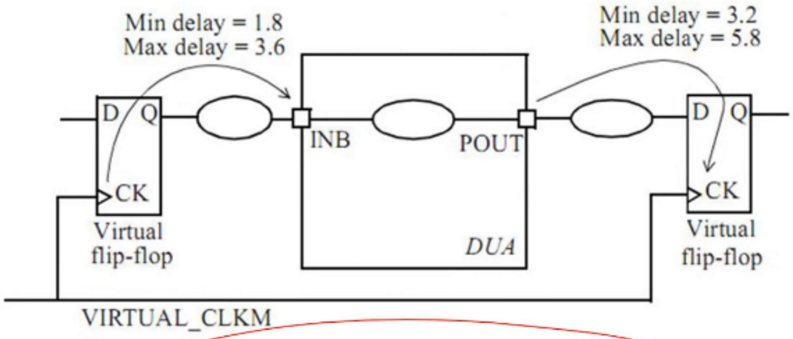
Hold Timing Check

3、Input to Output Path



Hold Timing Check

3、Input to Output Path




```
set_load -pin_load 0.15 [get_ports POUT]
set_output_delay -clock VIRTUAL_CLKM \
  -min 3.2 [get_ports POUT]
set_input_delay -clock VIRTUAL_CLKM \
  -min 1.8 [get_ports INB]
set_input_transition 0.8 [get_ports INB]
```

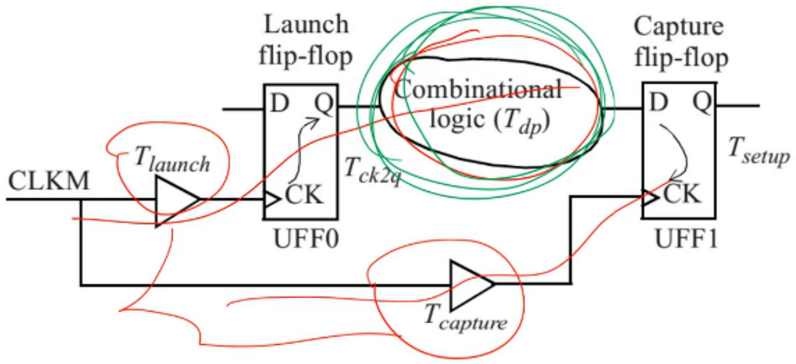
hold check if both input delays and output delays exist

Hold Timing Check

```
clock VIRTUAL_CLKM (rise edge)          0.00       0.00
clock network delay (ideal)             0.00       0.00
clock uncertainty                       0.05       0.05
output external delay                  -3.20      -3.15
data required time                                -3.15
-------------------------------------------------------
data required time                                -3.15
data arrival time                                 -2.12
-------------------------------------------------------
slack (MET)                                        5.27
```

对于max delay不满足setup check要求的情况，一般控制Tdq组合逻辑部分电路，使延迟降低

Conclusion-Setup Timing Check

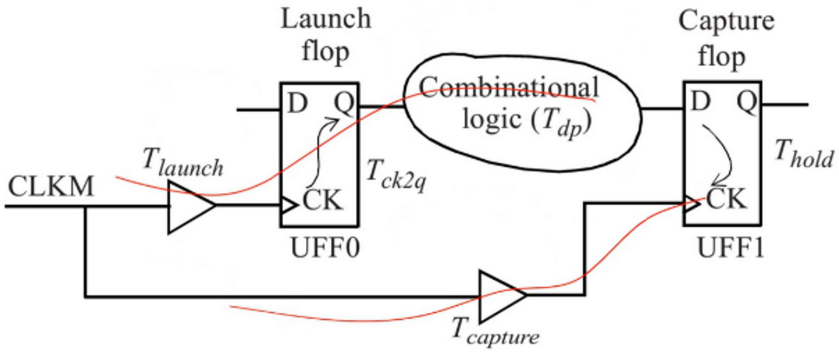


The setup check can be mathematically expressed as:

$$T_{launch} + T_{ck2q} + T_{dp} < T_{capture} + T_{cycle} - T_{setup}$$

min delay要比hold check要大，才能满足hold time要求

Conclusion-Hold Timing Check



The hold check can be mathematically expressed as:

$$T_{launch} + T_{ck2q} + T_{dp} > T_{capture} + T_{hold}$$