Next Generation IC Technology Challenges and Opportunities

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清华大学下一代芯片技术3DIC/Chiplet学术研讨会

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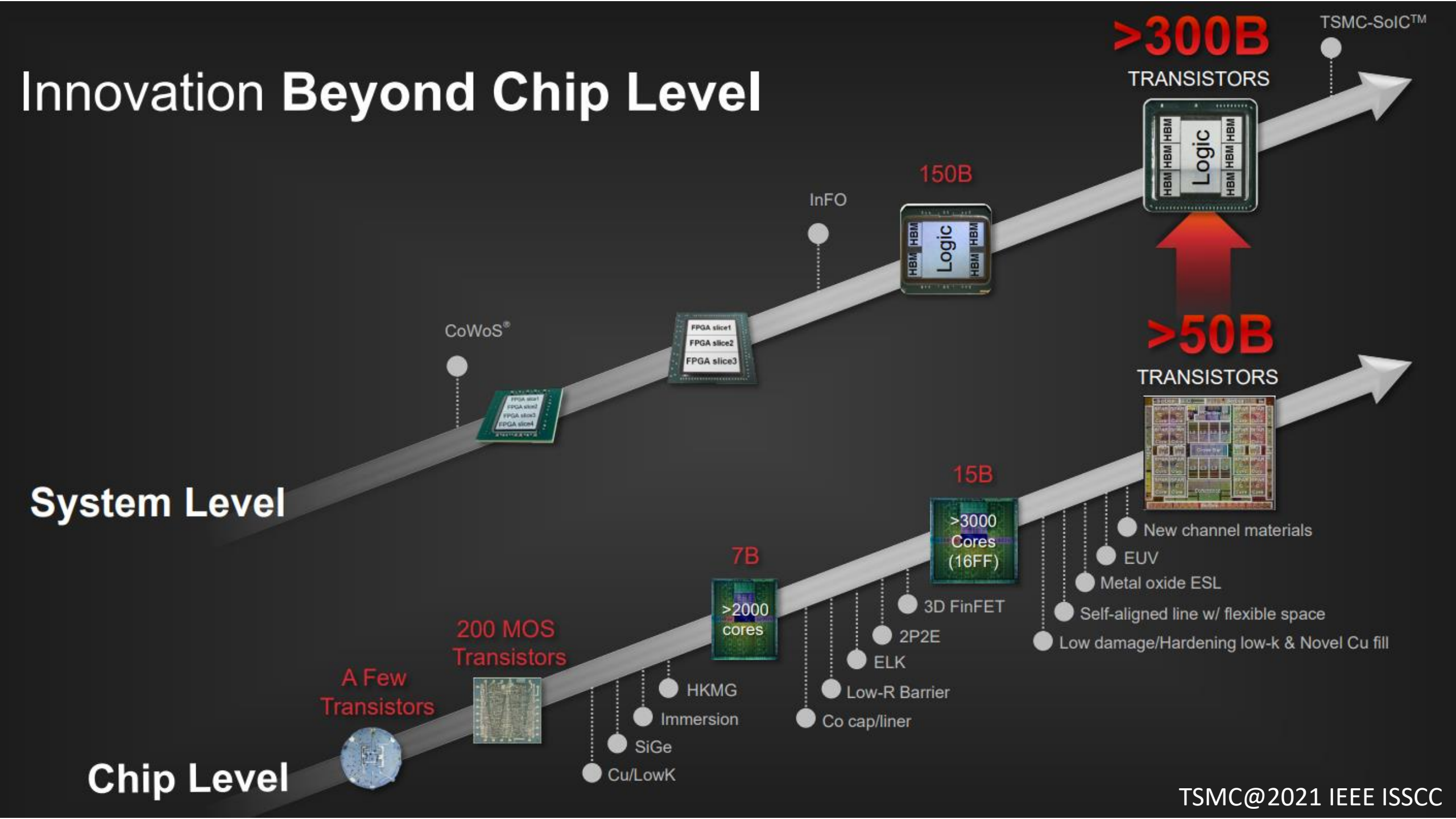
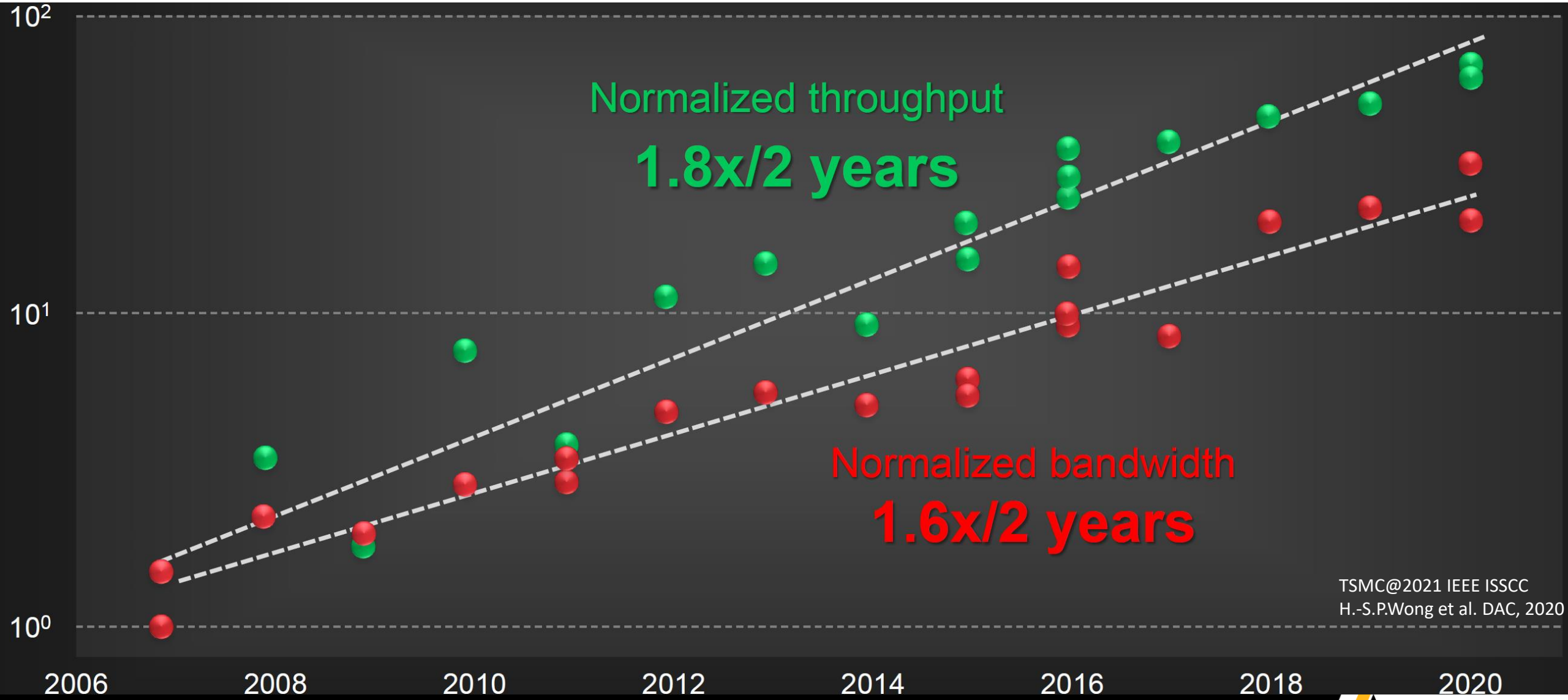
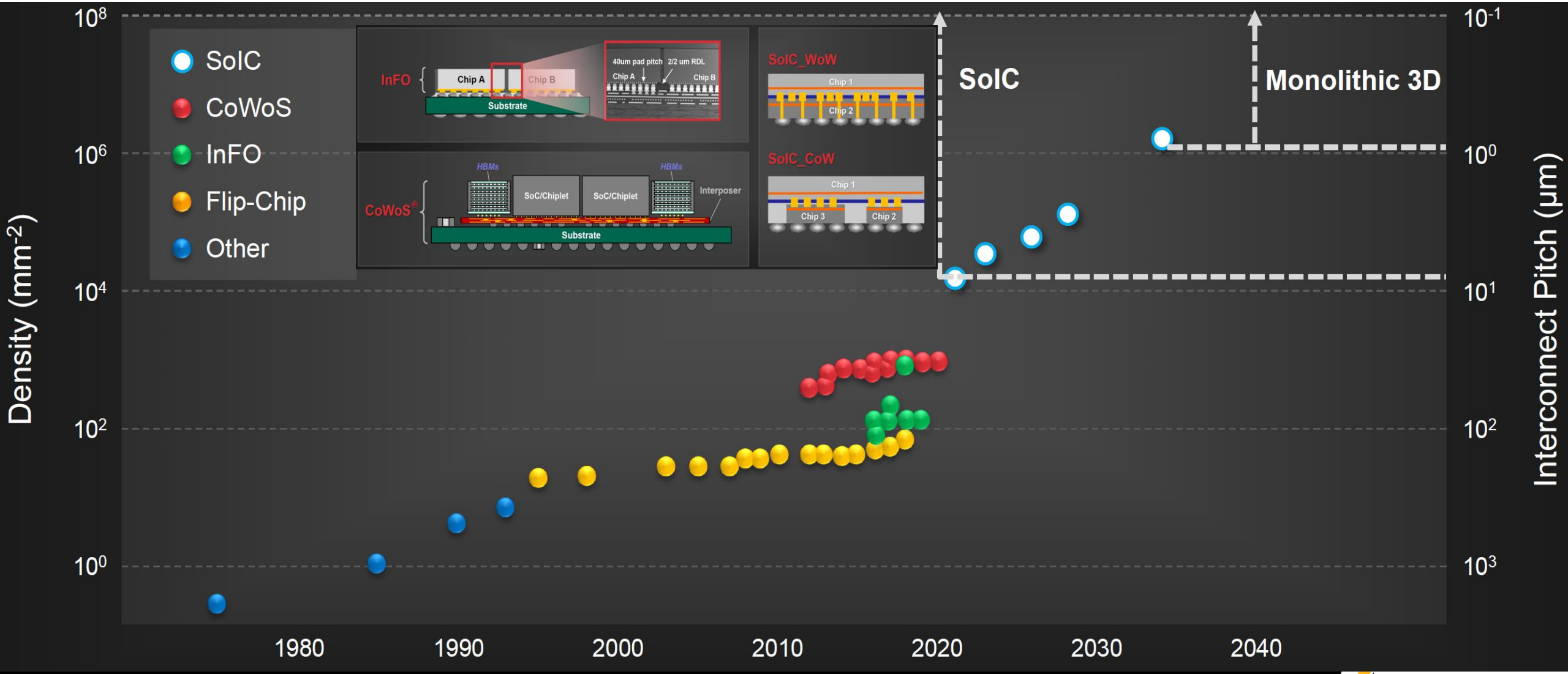
Innovation **Beyond Chip Level**



Bandwidth Deficit Limits System Throughput – MORE I/O DENSITY



Advanced Packaging for Another 10,000X I/O Density Increase



TSMC@2021 IEEE ISSCC

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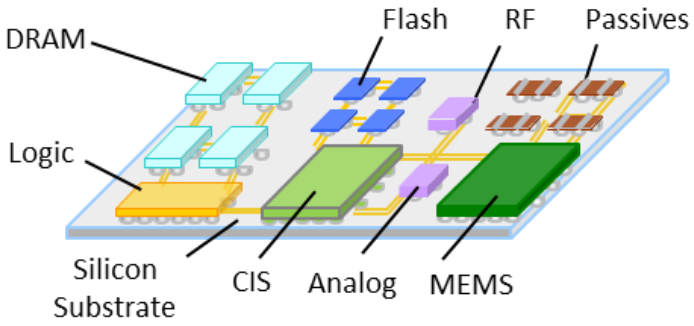
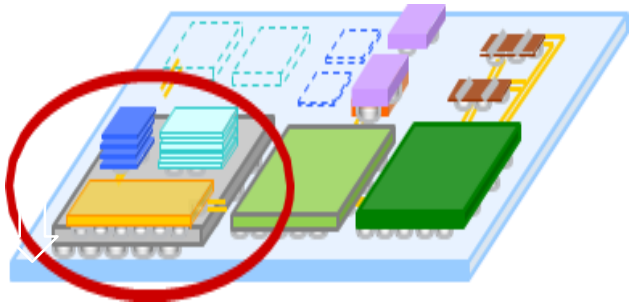
Pros and Cons of 3DIC/2.5DIC with Chiplet

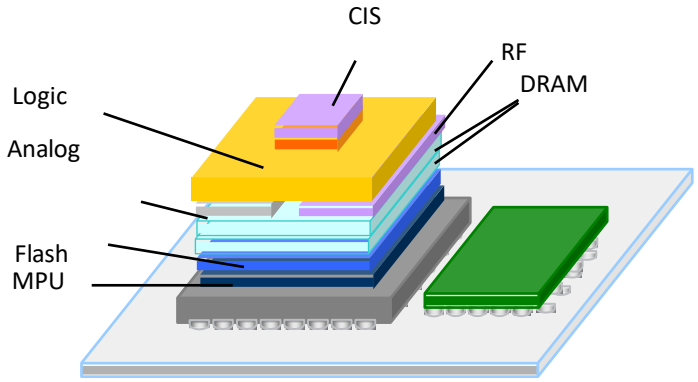
Building Chip like Modulized Software Programming!



Conventional 2D



2.5D (Silicon Interposer)



3D Stacked IC

Courtesy of TSMC Reference Flow

Pros	Cons
• Small form factor • Short channel length & propagation delay • Lower power, higher bandwidth • High system performance • With Chiplet: Reusable, higher yield, higher IO density/bandwidth	• Small heat sink area => Heat accumulation (Thermal) • Design implementation is hard • High complexity • Difficult to analyze, verify and signoff (and testing) • With Chiplet: More testing, Connection design/verification/manufacturing, thermal

Eco System for 2.5D/3D IC Power, Signal and Thermal Integrity

1. Modeling connectivity of complicated 3DIC structure
2. Parasitic modeling of packages (Interposer, FOWLP), board PCB
3. Power, signal and thermal modeling of interconnects of stacked dies
4. Noise source modeling for power, signal and thermal
5. Interface connection (Bump, Ball and TSV) modeling

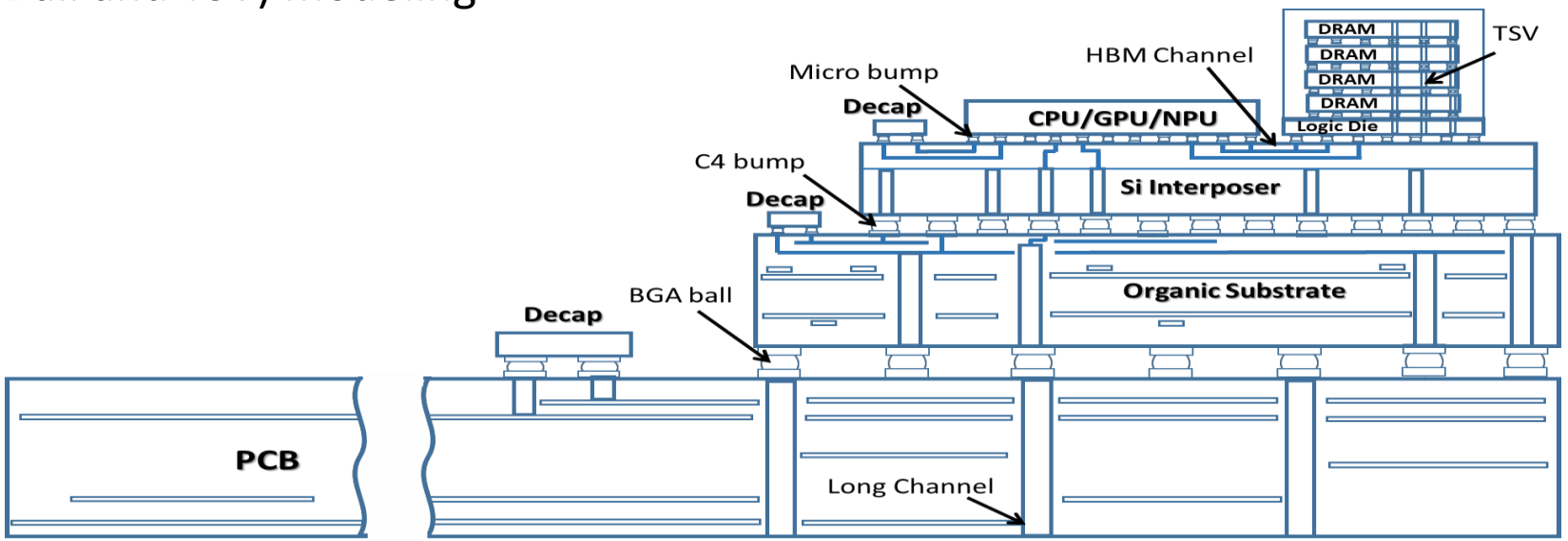
UCIe Universal Chiplet Interconnect Express

Modulized 3DIC Design
Chiplet with connections (TSMC)

Die + Bump + Interposer
CoWoS

Die + Cu Via + Interposer
InFO

Die + Cu Bond + Die
SoIC



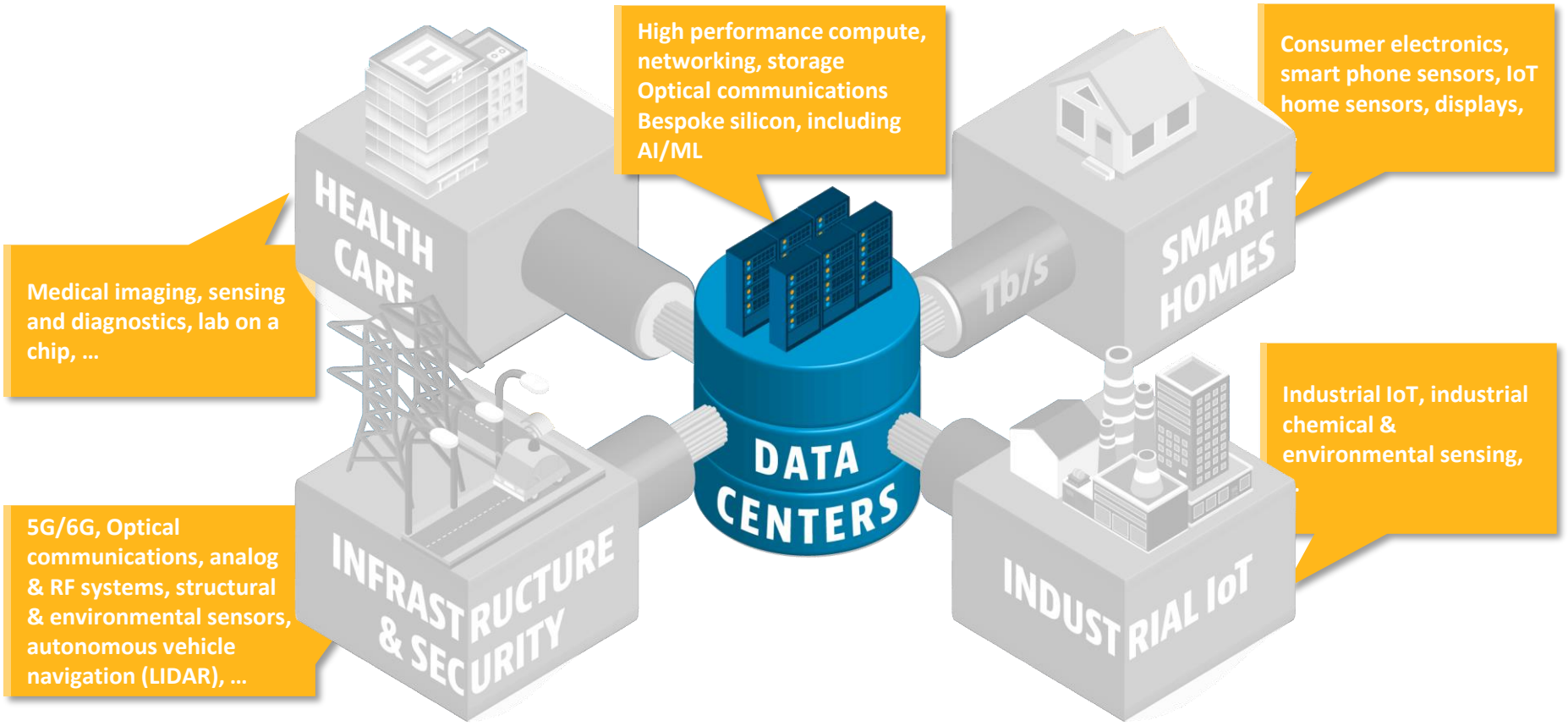
Wendem Beyene, "Power Delivery Network Design and Optimization for High-Speed Systems with Si Interposer", DesignCon 2017

Need for accurate and easy set up for chip, package and board co-simulation

Comprehensive chip, package and system co-design and co-analysis is necessary

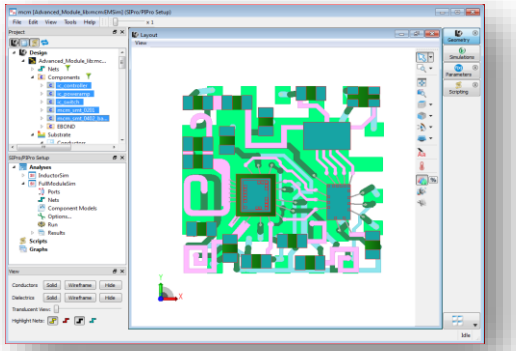
Ansys

Data – Key Driver For Information Society

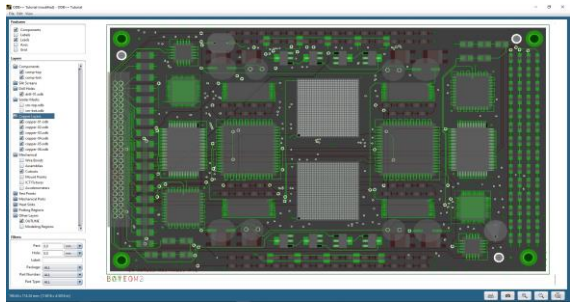


Data Sensing, Reception, Transmission and Processing
(**Electromagnetics, Optics, Electronics, Semiconductors**)

Integration Beyond Electronics and Semiconductors – w/ Optics



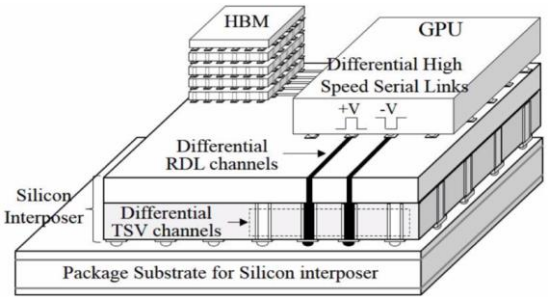
RF, PMIC, AMS



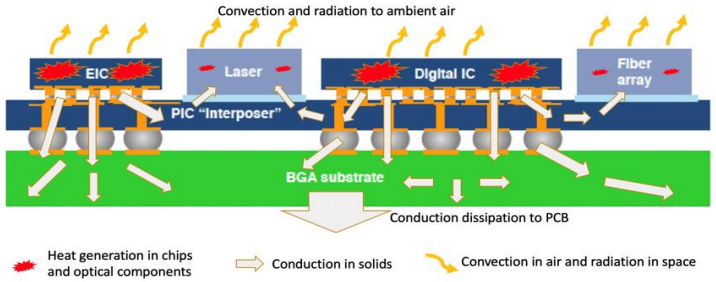
Chip-Package-Board

5G/6G and Edge IoT

HPC and Cloud

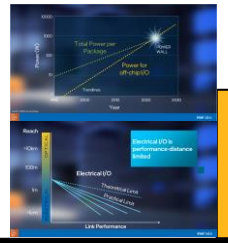


FinFET and 3D-IC

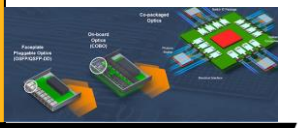


Co-packaged electro-optical

Automotive, Aerospace and Industrial



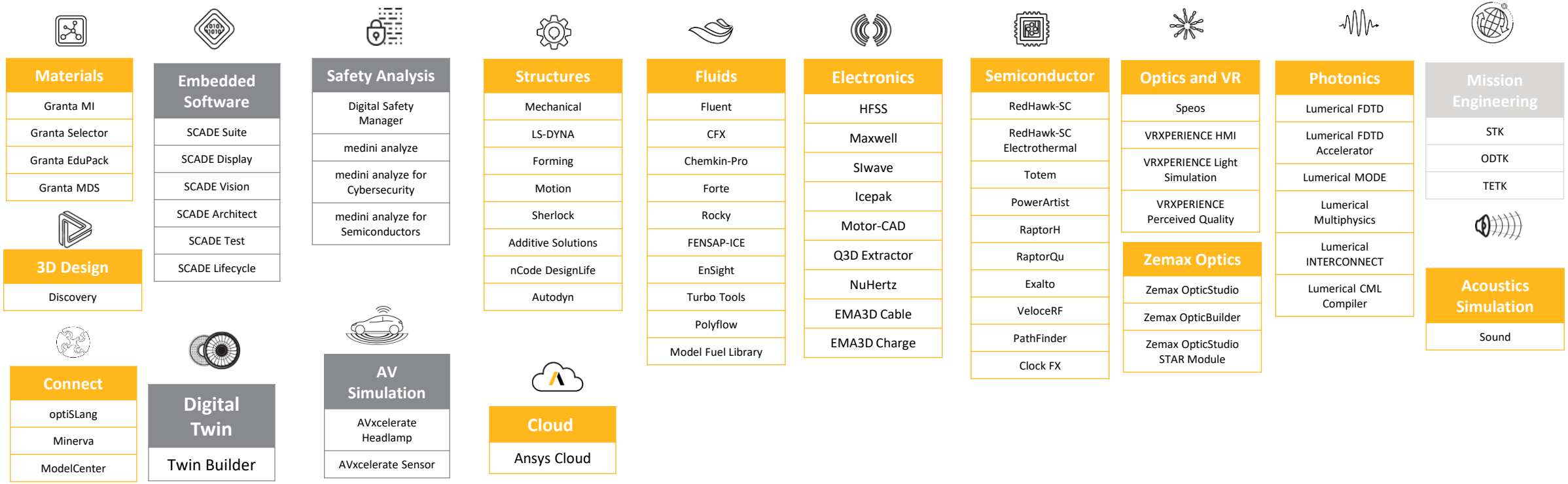
Multiphysics Solutions for SI/PI/TI/Reliability
(**Electromagnetics, Optics, Thermal**) x (Die, 3D-IC, Package, Board)



https://newsroom.intel.com/wp-content/uploads/sites/11/2020/12/2020_LabsDay_Keynote-slides.pdf

PowerPoint Presentation (ieee802.org)

Ansys – A Hub For Scientists and Engineers

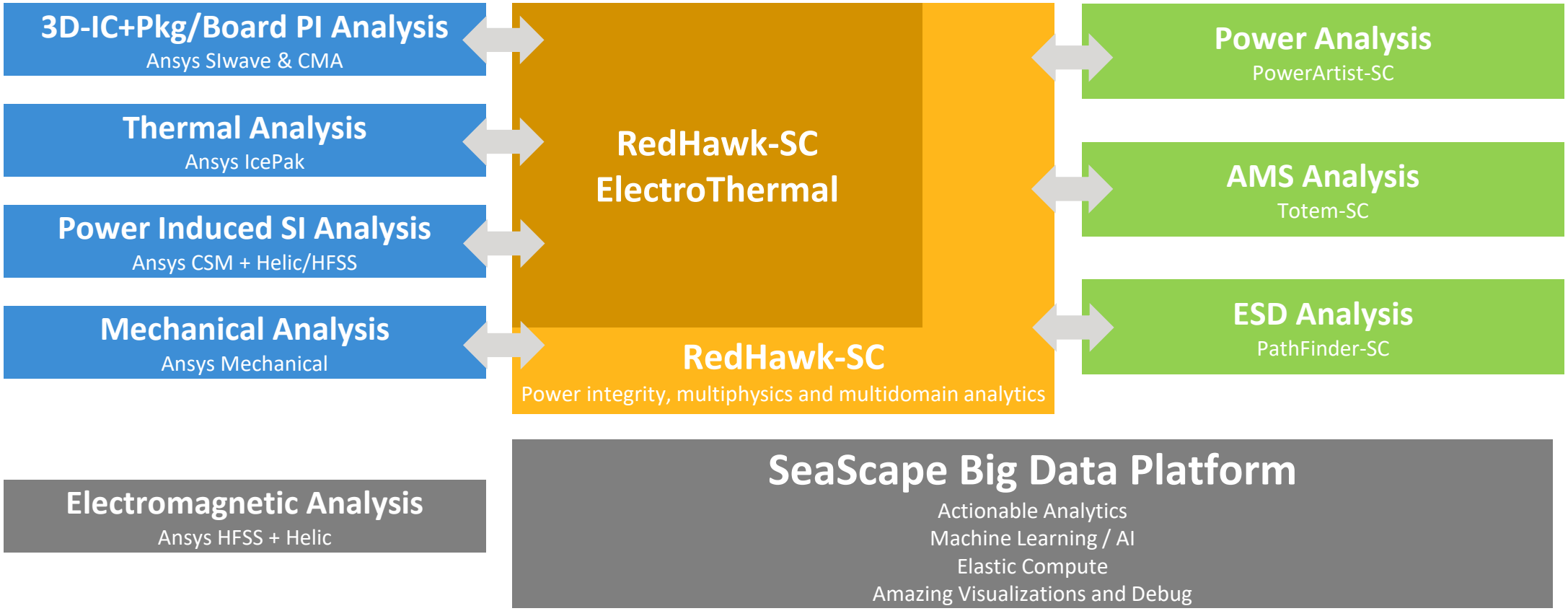


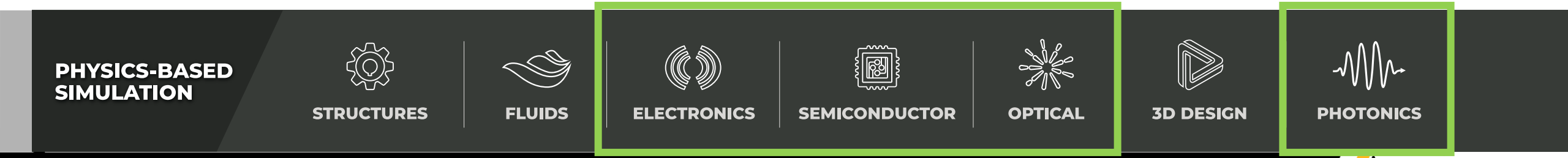
Ansys - one of the Big-4 EDA companies

Revenue: ~$2B EDA, major 3DIC/Chiplet Multiphysics solution provider

One of Four Major EDA companies for Leading Foundry Golden Solution Certification

Ansys SeaScape Platform for Chiplet/3DIC-Centric Multiphysics





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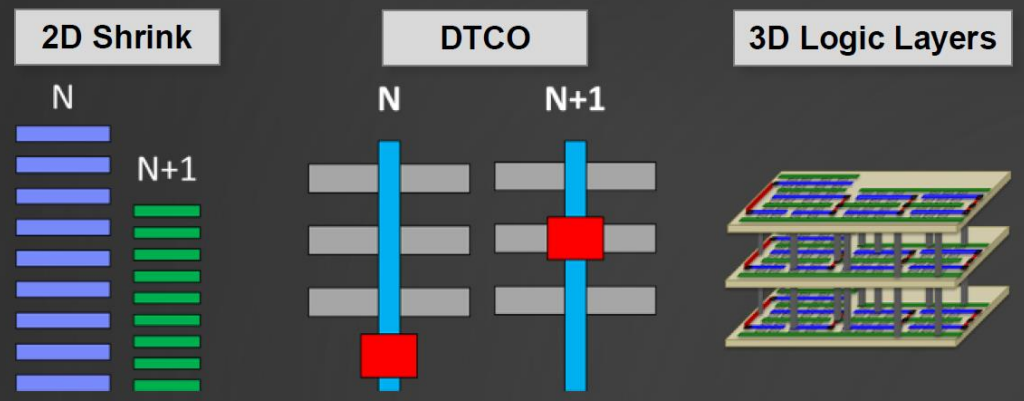
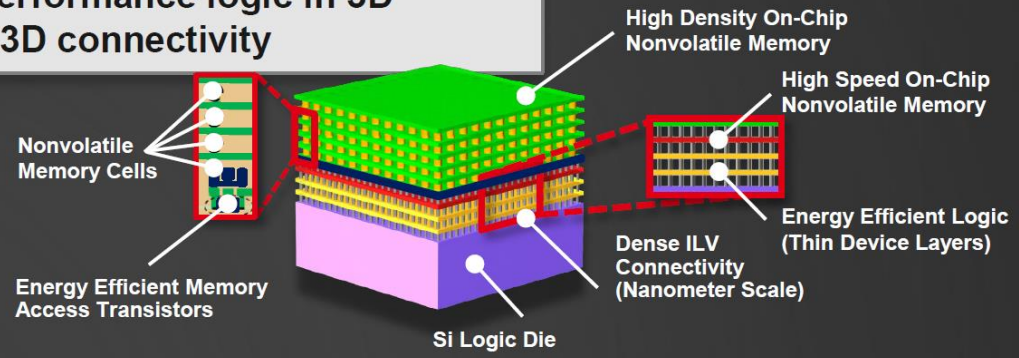
The Future is SYSTEM INTEGRATION



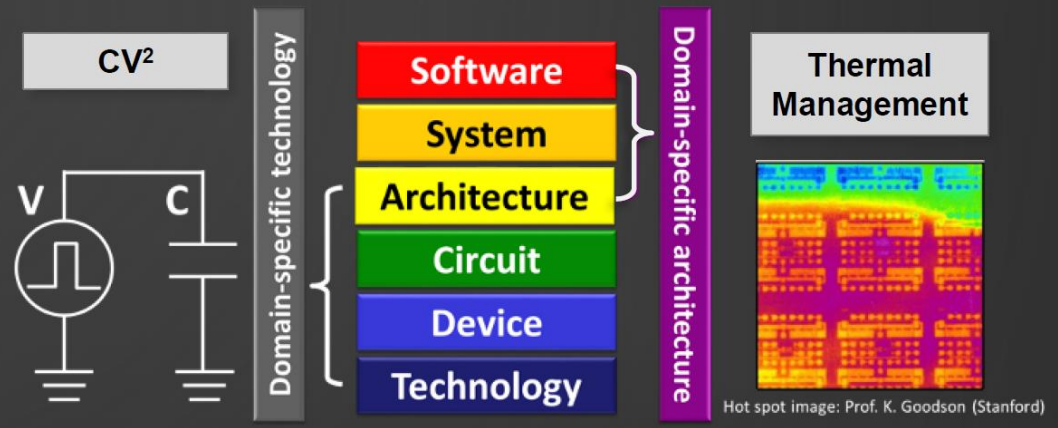
More transistors

- Local and optimized on-chip memory
- High-performance logic in 3D
- Dense 3D connectivity



More memory

Logic-memory integration



End-to-end optimization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