# Whole-Chip ESD Protection Design with Efficient VDD-to-VSS ESD Clamp Circuits for Submicron CMOS VLSI

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***Abstract*— A whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits is proposed to provide a real whole-chip ESD protection for submicron CMOS IC's without causing unexpected ESD damage in the internal circuits. The efficient VDD-to-VSS ESD clamp circuit has been designed to provide a low-impedance path between the VDD and VSS power lines of the IC during the ESD-stress condition, but this ESD clamp circuit is kept off when the IC is under its normal operating condition. Due to the parasitic resistance and capacitance along the VDD and VSS power lines, the ESD-protection efficiency is dependent on the pin location on a chip. Therefore, an experimental test chip has been designed and fabricated to build up a special ESD design rule for whole-chip ESD protection in a 0.8-$\mu$m CMOS technology. This whole-chip ESD protection design has been practically used to rescue a 0.8-$\mu$m CMOS IC product with a pin-to-pin HBM ESD level from the original level of 0.5 kV to become above 3 kV.**

***Index Terms*—ESD, ESD clamp circuit, snapback.**

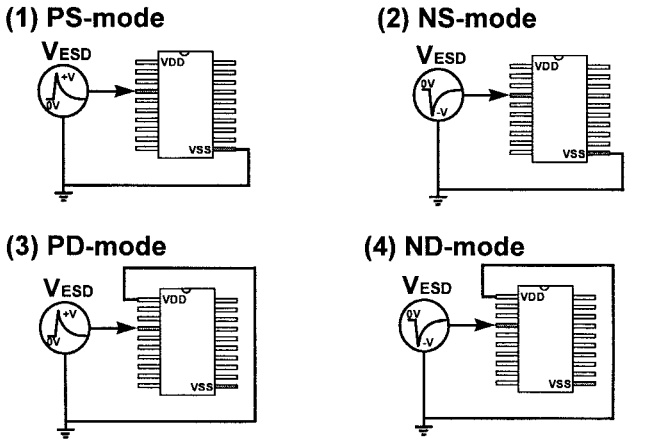


Fig. 1. Four modes of ESD stress on an input (or output) pin with respect to the grounded VDD or VSS pins.

## I. Introduction

ELECTROSTATIC DISCHARGE (ESD) protection has become an important task on the reliability of CMOS IC's. Especially in the submicron CMOS technologies, the advanced processes greatly degrade the ESD robustness of CMOS IC's [1], [2]. Besides the input or output ESD protection circuits placed around the input or output pads, some unexpected ESD damages are still found in the internal circuits of CMOS IC's beyond the input or output ESD protection circuits [3]–[11]. Even the parasitic capacitance and resistance along the power lines of the IC also causes a negative impact on the ESD reliability of the CMOS IC [9]–[11].

Since the ESD stress may have positive or negative voltage on an input (or output) pin with the VDD or VSS pins, respectively, grounded, there are four ESD-stress modes on an input (or output) pin [12]. The four modes of ESD stresses on the input or output pins are illustrated in Fig. 1. The input or output ESD protection circuits are therefore designed to bypass the ESD current from the stressed pin to the VDD or VSS pins. However, the ESD current may enter into any pin and go out from another pin of the IC. The ESD voltage may be applied across any two pins of the IC and cause some unexpected ESD damages in the internal circuits. Two additional ESD testing conditions, the pin-to-pin ESD stress and the VDD-to-VSS ESD stress, had been specified in the ESD testing standard to verify the whole-chip ESD reliability [12]. These two additional ESD testing conditions are illustrated in Fig. 2(a) and (b). In these two ESD testing conditions, the internal circuits are more vulnerable to ESD damage even if there are input and output ESD protection circuits in the IC's [13]–[15].

In the pin-to-pin ESD stress of Fig. 2(a), the ESD voltage across the pins can be conducted into the VDD or VSS power lines of the IC. The ESD current discharging paths in the IC under the pin-to-pin ESD stress condition are illustrated in Fig. 3. In Fig. 3(a), a positive ESD voltage is applied to an input pin with some output pin relatively grounded, but both the VDD and VSS pins are floating. Before the positive ESD voltage on the input pad is discharged through the input protection diode Dn1, the ESD current is conducted into the floating VDD power line through the forward-biased diode Dp1 in the input ESD protection circuit. The ESD current is therefore conducted into the internal circuits through the VDD power line and discharged through the internal circuits to VSS. In Fig. 3(b), a negative ESD voltage is applied to an output pin, while some input pin is grounded but the VDD and VSS are floating. Such negative ESD voltage is also conducted into the internal circuits through the VSS power line of the IC. In the VDD-to-VSS ESD testing condition of Fig. 2(b), the ESD voltage is directly applied to the VDD pin with the VSS

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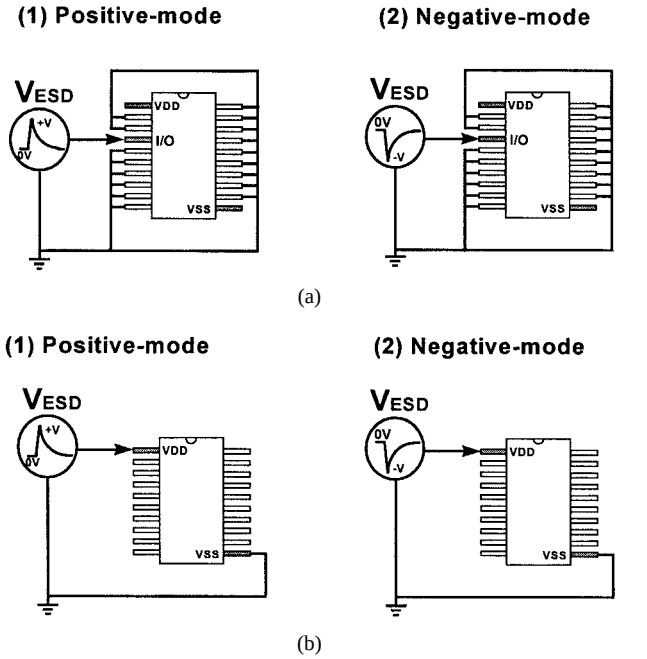



Fig. 2. Two additional ESD-testing conditions to verify the whole-chip ESD reliability. (a) The pin-to-pin ESD stress: the ESD voltage is applied to an input (or output) pin while all other input and output pins are grounded but the VDD and VSS pins are floating. (b) The VDD-to-VSS ESD stress: the ESD voltage is directly applied to the VDD pin with the VSS pin grounded but all input and output pins are floating.

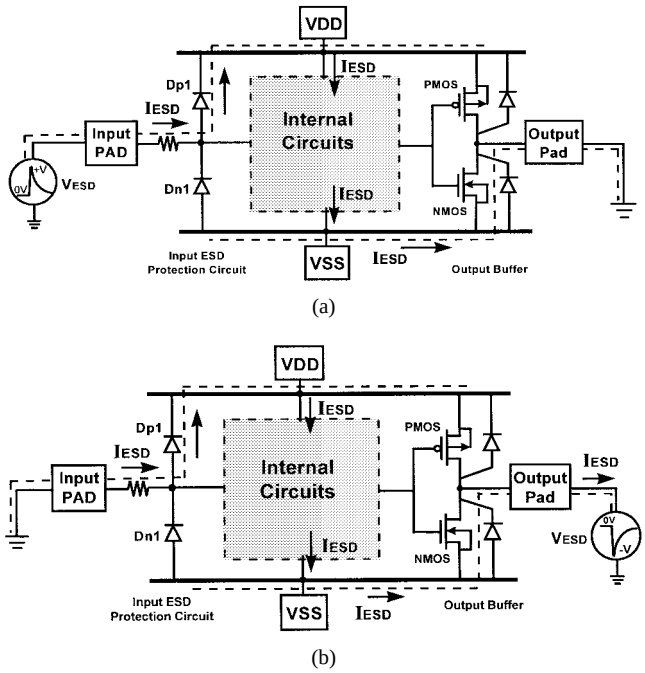



Fig. 3. ESD current paths through the IC under the pin-to-pin ESD testing condition. (a) A positive ESD voltage is applied to some input pin while another output pin is grounded. (b) A negative ESD voltage is applied to some output pin while another input pin is grounded.

pin grounded but all the input and output pins are floating. The ESD current discharging path in this VDD-to-VSS ESD stress condition is illustrated in Fig. 4. Because the internal circuits are often drawn with the minimum device dimensions and layout spacings to save layout area, the internal circuits are very vulnerable to the ESD current. The ESD damages in the internal circuits are difficult to be found by only measuring the leakage current on the input or output pins. Complex failure analyzes with full function verification are often required to find the failure location.

In order to clamp the ESD overstress voltage across the power lines, the gate-grounded NMOS was used as the ESD clamp device between the VDD and VSS power lines [7]–[9], [14], [15], as shown in Fig. 5. In the pin-to-pin or the VDD-to-VSS ESD stresses, the ESD voltage across the VDD and VSS power lines of the IC is clamped by the gate-grounded NMOS in its snapback-breakdown region. Because the ESD current is discharged through the gate-grounded NMOS, this gate-grounded NMOS has to be drawn with a larger device dimension to protect itself. However, the device dimensions and layout spacings of the internal circuits are further reduced in the scaled-down CMOS technology. During the pin-to-pin or the VDD-to-VSS ESD stresses, the internal circuits with minimum device dimensions and spacings are easily damaged by the ESD overstress voltage before the gate-grounded NMOS with larger device dimension is broken down to bypass the ESD current. So, to really protect all the circuits in an IC, a suitable ESD clamp circuit has to be placed between the VDD and VSS power lines of the IC to clamp the ESD overstress voltage across the power lines [16]–[20].

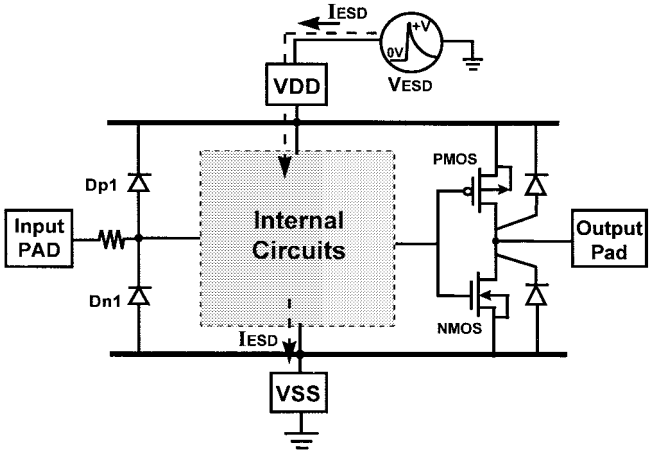



Fig. 4. ESD-current discharging path through the IC under the VDD-to-VSS ESD testing condition.

However, when more functions and circuits are integrated into a single chip, the die size of a CMOS IC is enlarged with longer VDD and VSS power lines surrounding the whole chip. The longer power lines can cause a delay to discharge ESD current through the desired ESD clamp circuit in the CMOS VLSI [9]–[11]. This causes that the ESD levels of different pins are dependent on their pin locations in the chip. If the ESD-stressed pin is far from the desired VDD-to-VSS ESD clamp circuit, the ESD current can be still conducted into the internal circuits to cause some unexpected ESD damages in the internal circuits.

In this paper, the dependence of ESD level on different pin location is investigated by an experimental test chip. Therefore, a whole-chip ESD protection design with efficient

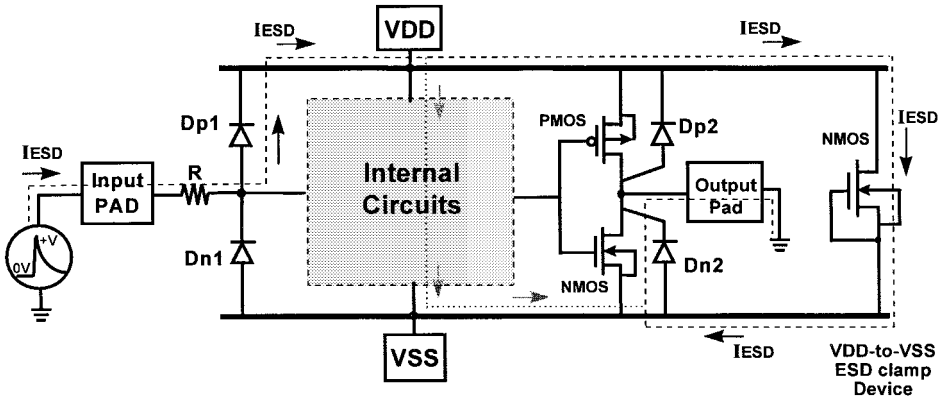



Fig. 5. Prior art of VDD-to-VSS ESD protection design by using a gate-grounded NMOS as the ESD clamp device between the VDD and VSS power lines.

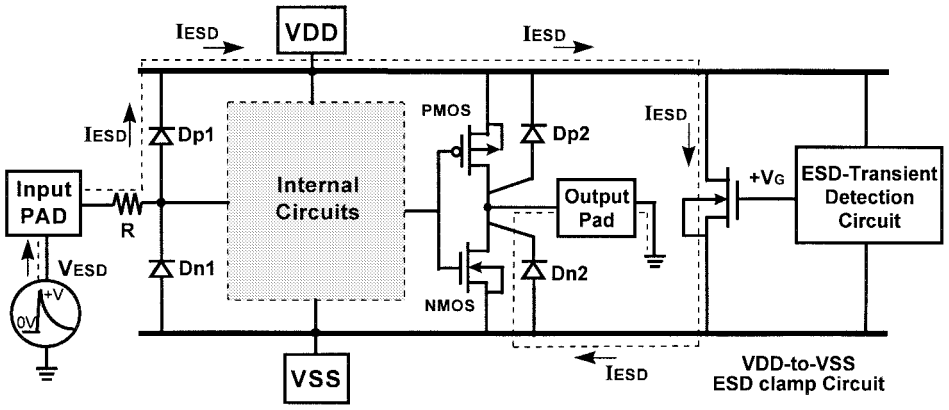



Fig. 6. An effective VDD-to-VSS ESD protection design to achieve the whole-chip ESD protection.

VDD-to-VSS ESD clamp circuits is demonstrated to fully protect a submicron CMOS IC without causing unexpected ESD damage in the internal circuits [21]. This whole-chip ESD protection design has been successfully implemented in a mass-production consumer IC to improve its human-body-model (HBM) ESD level from 0.5 to above 3 kV in all ESD testing conditions, but without increasing the die size of the IC product.

## II. Efficient VDD-To-VSS ESD Clamp Circuit

### A. Concept of the Efficient ESD Clamp Circuit

To efficiently clamp the ESD voltage across VDD and VSS power lines before the internal circuits are damaged, an ESD-transient detection circuit is used to turn on the VDD-to-VSS ESD-clamping NMOS, as illustrated in Fig 6. The ESD-transient detection circuit is designed to detect the ESD event and sends a control voltage to the gate of the ESD-clamping NMOS. Because the ESD-clamping NMOS is turned on by a positive gate voltage rather than by the drain snapback-breakdown, the NMOS can be turned on at lower voltage to bypass the ESD current before the internal circuits are damaged by the ESD overstress voltage. In the pin-to-pin ESD stress condition, as shown in Fig. 6, the ESD current is diverted from the input pin into the floating VDD power line. The floating VSS power line is initially biased at a ground level through the parasitic diode Dn2 in the output NMOS with a grounded output pin. Therefore, the ESD-transient detection circuit is biased by the ESD energy and turns on the ESD-clamping NMOS to provide a low-impedance path between the VDD and VSS power lines to bypass ESD current. Thus, the ESD current can be efficiently discharged through the forward-biased diode Dp1, the ESD-clamping NMOS, and the diode Dn2. The devices operating in the forward-biased conditions can sustain much higher ESD current than they operating in the reverse-biased breakdown conditions. But, when the IC is in the normal operating condition with the power supplies, this ESD-clamping NMOS has to be kept off to avoid power loss from VDD to VSS.

### B. Realization of the ESD Clamp Circuit

To realize the aforementioned ESD-transient detection function, a $RC$-based VDD-to-VSS ESD clamp circuit is shown in Fig. 7. This ESD clamp circuit is designed to be turned on when the ESD voltage appears across the VDD and VSS power lines. But, this ESD clamp circuit is kept off when the IC is under the normal power-on condition. To meet these requirements, the $RC$ time constant in the VDD-to-VSS ESD clamp circuit is designed about 0.1–1 $\mu$s to achieve the desired operations.

Initially, the nodes $V_x$ and $V_G$ have the voltage levels the same as the VSS level because the IC is in the floating condition without power supplies. The ESD voltage across the VDD and VSS power line will charge the capacitor $C$ to

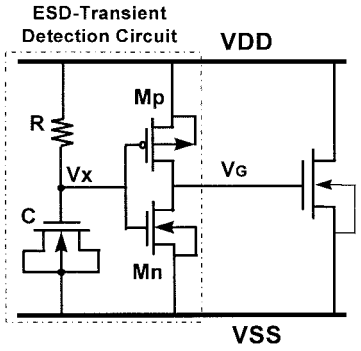
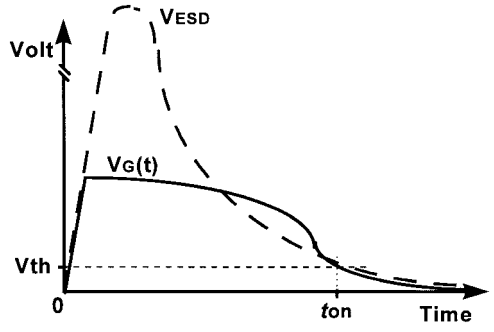
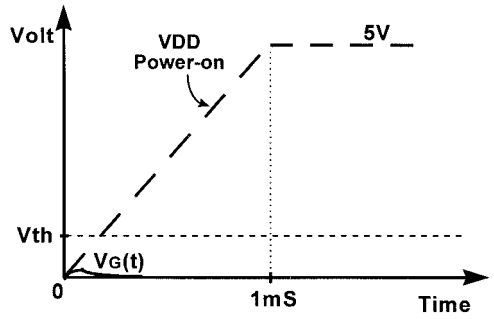



Fig. 7. Realization of the efficient VDD-to-VSS ESD clamp circuit.



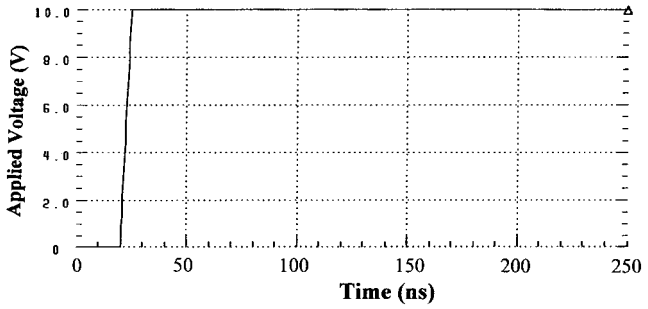

(a)



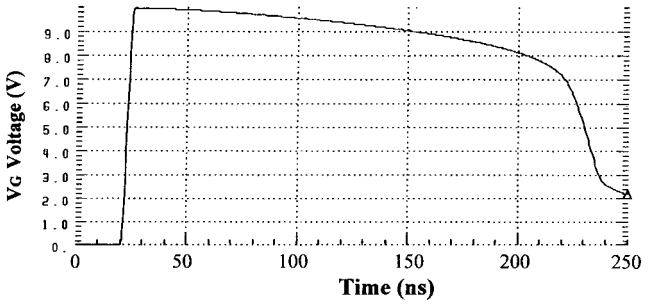

(b)

Fig. 8. Schematic voltage waveform on the node $V_G$ in Fig. 7 under (a) the ESD-stress condition and (b) the normal power-on condition.

rise up the voltage level of $V_x$ in Fig. 7. The ESD voltage has a rise time about ~10 ns [12]. The voltage level of $V_x$ is increased much slower than the voltage level on the VDD power line, because the $RC$ circuit has a time constant in the order of microsecond ($\mu$s). Due to the delay of the voltage increase on the node $V_x$, the $M_p$ device is biased by the ESD voltage and conducts a voltage into the node $V_G$ to turn on the ESD-clamping NMOS. The turned-on NMOS, which provides a low-impedance path between the VDD and VSS power lines, can clamp the ESD voltage across the VDD and VSS power lines. So, the internal circuits can be effectively protected without ESD damage. A schematic voltage waveform on the node $V_G$ under the ESD-stress condition is shown in Fig. 8(a). The turn-on time ($t_{\rm on}$) of the ESD-clamping NMOS can be mainly adjusted by the $RC$ time constant in the ESD-transient detection circuit. The turn-on time of the ESD-clamping NMOS is designed about 200 ns to meet the half-energy discharging time of the HBM ESD event [12].

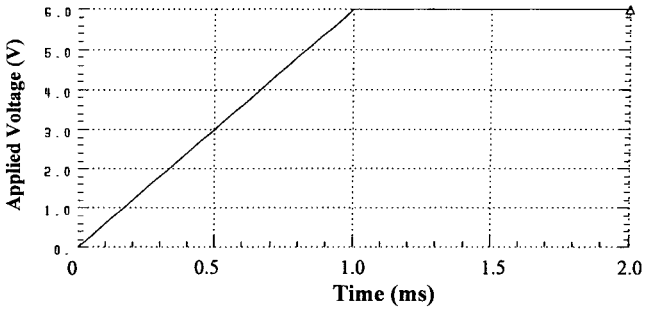



(a)

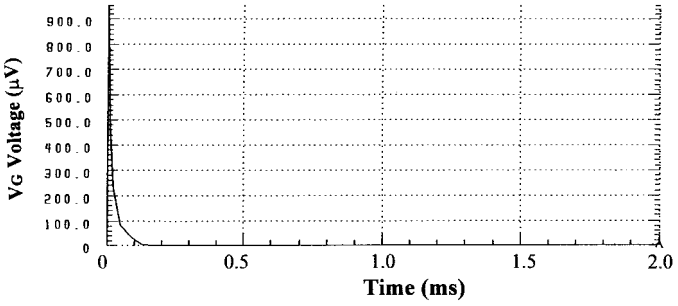



(b)

Fig. 9. $HSPICE$ simulated voltage waveforms in the ESD-stress condition: (a) a ramp voltage with a rise time of 10 ns to simulate the rising edge of an HBM ESD pulse and (b) the simulated voltage waveform on the node $V_G$ when the ramp voltage in (a) is applied to VDD.



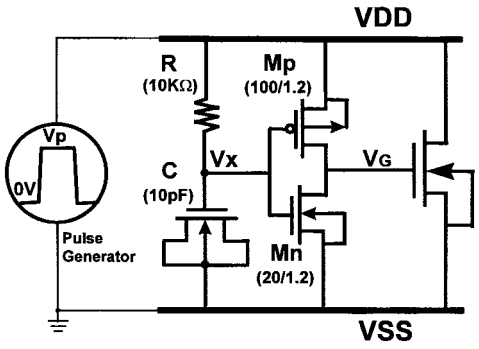

(a)



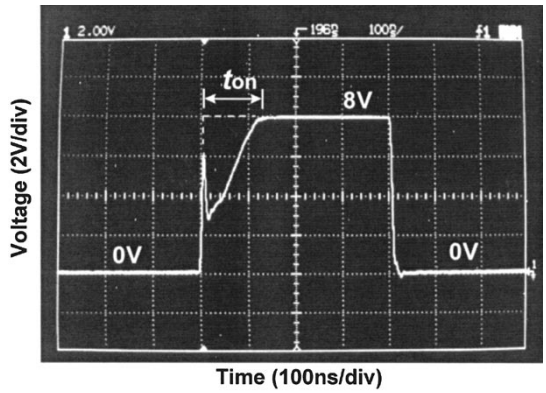

(b)

Fig. 10. $HSPICE$ simulated voltage waveforms in the VDD power-on condition: (a) a ramp voltage with a rise time of 1 ms to simulate the VDD power-on voltage and (b) the simulated voltage waveform on the node $V_G$ when the VDD power-on voltage in (a) is applied to VDD.

Under the normal VDD power-on condition, the VDD power-on voltage waveform has a rise time in the order of millisecond (ms). With such a slow rise time of ms, the voltage level on the node $V_x$ in the ESD-transient detection circuit with

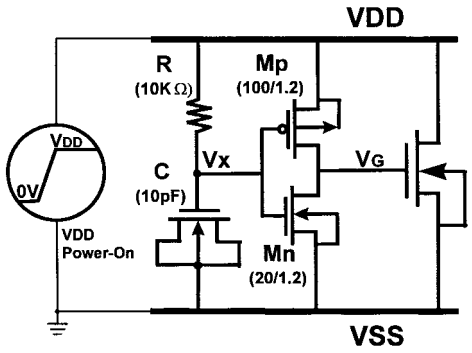



(a)

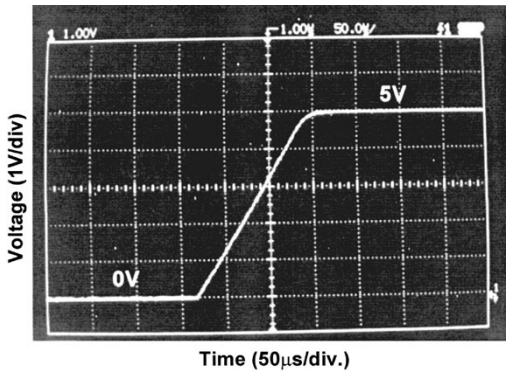



(b)

Fig. 11. Turn-on verification on the proposed VDD-to-VSS ESD clamp circuit in the ESD-stress condition: (a) the experimental setup used to simulate the ESD-stress condition and (b) the measured voltage waveform on the VDD power line.




(a)




(b)

Fig. 12. Turn-on verification on the proposed VDD-to-VSS ESD clamp circuit in the VDD power-on condition: (a) the experimental setup used to simulate the normal VDD power-on condition and (b) the measured voltage waveform on the VDD power line.

a $RC$ time constant of $\mu$s can follow the VDD voltage in time to keep the $M_p$ off. Because the $V_x$ is simultaneously increased to the VDD voltage level in the VDD power-on condition, the $M_n$ is turned on to keep the $V_G$ at a voltage level of 0 V. So, the ESD-clamping NMOS is guaranteed to be kept off when the IC is under the VDD power-on condition or in the normal operating conditions. The schematic voltage waveform of $V_G$ in the time domain under the VDD power-on condition is illustrated in Fig. 8(b). The $V_G$ maybe has a little glitch when the VDD just rises up, but the glitch of $V_G$(t) can be below the NMOS threshold voltage to keep the ESD-clamping NMOS always off during the VDD power-on transition.

Due to the difference in the rise times between the ESD voltage and the VDD power-on voltage, the VDD-to-VSS ESD clamp circuit provides a low-impedance path between VDD and VSS power lines in the ESD-stress conditions, but it becomes a open circuit between the power lines in the VDD power-on condition. To actually meet the aforementioned operations, the circuit simulation program $HSPICE$ is used to find the suitable $RC$ value and device sizes for this VDD-to-VSS ESD clamp circuit. The device dimensions for this ESD-transient detection circuit in a typical 0.6-$\mu$m CMOS process are chosen as $R = 10$ k$\Omega$, $C = 10$ pF, $W/L$ of $M_p = 100/1.2$, and $W/L$ of $M_n = 20/1.2$. The resistor $R$ of 10 k$\Omega$ is realized by an N-well resistance, and the capacitor of 10 pF is realized by an NMOS device with a device dimension ($W/L$) of $48/40$ ($\mu$m/$\mu$m) in the 0.6-$\mu$m CMOS process. The $HSPICE$ simulated voltage waveforms in the time domain at the node $V_G$ during the ESD-stress condition and the normal VDD power-on condition are shown in Figs. 9 and 10, respectively. In Fig. 9(a), a ramp voltage with a rise time of 10 ns is used to simulate the rising edge of an HBM ESD pulse. Because the NMOS snapback-breakdown voltage is about 12 V in the 0.6-$\mu$m CMOS process, the pulse height of the ramp voltage is set as 10 V to monitor the voltage on the node $V_G$ before the ESD-clamping NMOS is broken down. As shown in Fig. 9(b), the voltage waveform on the node $V_G$ is simultaneously increased when the ramp voltage is applied to VDD, whereas the VSS is grounded. By changing the $RC$ time constant, the turn-on time of the ESD-clamping NMOS can be adjusted. In Fig. 10(a), a VDD power-on voltage waveform with a rise time of 1 ms and a voltage height of 6 V is applied to the VDD line of the ESD clamp circuit. During such a VDD power-on condition, the voltage waveform on the node $V_G$ is shown in Fig. 10(b), where the $V_G$ peak voltage is only about 0.96 mV which appears in the initial time period. With a $V_G$ voltage as that shown in Fig. 10(b), the ESD-clamping NMOS can be always kept off when the IC is in the normal operation conditions.

The device dimension of the ESD-clamping NMOS is designed as large as possible to provide a much low turn-on resistance between the VDD and VSS power lines to quickly bypass the ESD current. But, an NMOS with a large device dimension also occupies a larger layout area. So, the device

dimension of the ESD-clamping NMOS is strongly dependent on the required ESD level and the specified layout area of the IC. For an IC product with a higher ESD specification, it needs a larger ESD-clamping NMOS to protect the internal circuits of the IC and itself.

### C. Turn-On Verification of the ESD Clamp Circuit

The VDD-to-VSS ESD clamp circuit had been fabricated in a 0.6-$\mu$m single-poly double-metal CMOS process. To verify the aforementioned ESD-transient detection function, an experimental setup is shown in Fig. 11(a), where a voltage pulse generated from a pulse generator (Hp 8116) is used to simulate the HBM ESD pulse. The voltage pulse generated from the pulse generator initially has a square-type voltage waveform with a rise time about 5 ns. When the voltage pulse is applied to the VDD power line with the VSS grounded, the sharp-rising edge of the ESD-like voltage pulse will trigger on the ESD-clamping NMOS to provide a low-impedance path between the VDD and VSS power lines. Due to the limited driving current of the pulse generator, the voltage waveform on the VDD power line will be degraded by the turned-on ESD-clamping NMOS. The degraded voltage waveform on the VDD power line is shown in Fig. 11(b), where a voltage pulse with a pulse height of 8 V and a pulse width of 400 ns is applied to the VDD power line. The voltage waveform is degraded at the rising edge because the ESD-clamping NMOS is simultaneously turned-on when the ESD-like voltage pulse is applied to the VDD power line. The voltage degradation is dependent on the turned-on resistance of the ESD-clamping NMOS and the output resistance of the pulse generator. The maximum voltage drop from the 8-V voltage level in Fig. 11(b) is 5.2 V. A larger device dimension of the ESD-clamping NMOS leads to a more serious degradation on the voltage waveform. When the node $V_x$ is charged up greater than the logic threshold voltage of the inverter ($M_p$ and $M_n$) in the ESD-transient detection circuit, the ESD-clamping NMOS will be turned off and the voltage waveform will be restored to the original voltage level. In Fig. 11(b), the applied 8-V voltage pulse has a recovery period about 135 ns, which is corresponding to the turn-on time of the ESD-clamping NMOS.

The turn-on time of the ESD-clamping NMOS is also dependent on the voltage level of the applied voltage pulse. A higher voltage pulse applied to the VDD power line leads to a larger $V_G$ voltage and a longer turn-on time on the ESD-clamping NMOS. In Fig. 7, the $V_G$ voltage will be simultaneously increased to the voltage level on VDD power line when the $M_p$ device is turned on during the ESD-stress condition. When the $V_G$ voltage level is increased higher than the snapback-breakdown voltage of the $M_n$ device, the $V_G$ voltage is clamped by the snapback-breakdown $M_n$ device to near its snapback holding voltage of 10 V in the 0.6-$\mu$m CMOS process.

With a gate voltage of 10 V, the ESD-clamping NMOS can be quickly triggered into its snapback region to bypass the ESD current from VDD to VSS power lines. But, an NMOS device with a higher gate voltage or a longer turn-on time often causes a lower $I_{t2}$ (secondary breakdown current) value [22], [23], because a shallow current flows through the channel surface of the NMOS. Thus, the ESD-clamping NMOS were designed with a large device dimension of 8000/0.8 in [16] to sustain an HBM ESD level of 3 kV. In the advanced submicron CMOS technology with silicided diffusion and LDD structure, the ESD-clamping NMOS has better to be drawn with the silicide-blocking mask, the ESD-implant mask, and a wider layout spacing from the drain contact to its ploy gate to improve its ESD-sustained level. In other design to increase the ESD-sustained level of the ESD-clamping NMOS, an N-well resistor was added into the drain region of the ESD-clamping NMOS in the VDD-to-VSS ESD clamp circuit [24]. In order to avoid the gate-driven effect [23] which causes a low ESD level on the NMOS device, and also to reduce the device dimension and layout area for the ESD-clamping device between VDD and VSS power lines, a substrate-triggering technique has been applied to trigger on a field-oxide device to provide a more area-efficient design for VDD-to-VSS ESD clamp circuit [25].

To verify the action of the VDD-to-VSS ESD clamp circuit in the normal VDD power-on condition, an experimental setup is shown in Fig. 12(a). A ramp voltage with a rise time of 0.1 ms and a high-level voltage of 5 V is applied to the VDD power line with the VSS power line grounded to simulate the VDD power-on condition. The voltage waveform on the VDD power line is monitored and shown in Fig. 12(b), where the voltage waveform is still remained as a ramp voltage without any degradation on the waveform. So, the ESD-clamping NMOS in the VDD-to-VSS ESD clamping circuit has been verified to be indeed kept off in the VDD power-on condition. This ESD clamping circuit can be always kept off while the IC is in the normal operating condition with the static VDD power supply.

## III. Whole-Chip ESD Protection Design

The operation of pin-to-pin ESD protection with the efficient VDD-to-VSS ESD clamp circuit has been explained in Fig. 6. With suitable design on the ESD-transient detection circuit, the ESD-clamping NMOS can provide an effective discharging path between VDD and VSS power lines to bypass ESD current away from the internal circuits of the IC. However, the modem VLSI (or ULSI) often has a very large die size, which has much longer VDD and VSS power lines to surround the whole chip and to connect the I/O circuits. Such longer power lines had been reported to have a negative impact on the ESD protection of IC's [9]–[11]. The negative impact on the pin-to-pin ESD protection owing to the longer VDD and VSS power lines is illustrated in Fig. 13, where the VDD-to-VSS ESD clamp circuit is placed far from the stressed input and output pads. The longer VDD and VSS power lines generally cause higher series resistance ($R_{dd}$ and $R_{ss}$) along the power lines or a larger VDD-to-VSS parasitic capacitance ($C_{ds}$) across the power lines. The parasitic $R_{dd}$, $R_{ss}$, and $C_{ds}$ along the VDD and VSS power lines contribute a time delay to limit the ESD current discharging through the ESD-clamping NMOS. The equivalent parasitic $R_{dd}$, $R_{ss}$, and $C_{ds}$ along the VDD and VSS power lines are strongly dependent on the location of the

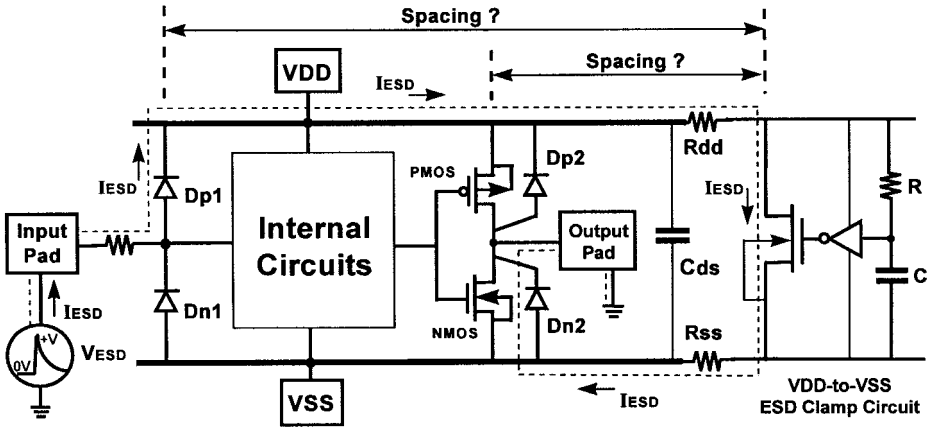



Fig. 13. Schematic diagram to show the spacing effect on the ESD protection of a chip due to the parasitic resistance and capacitance along the VDD and VSS power lines.

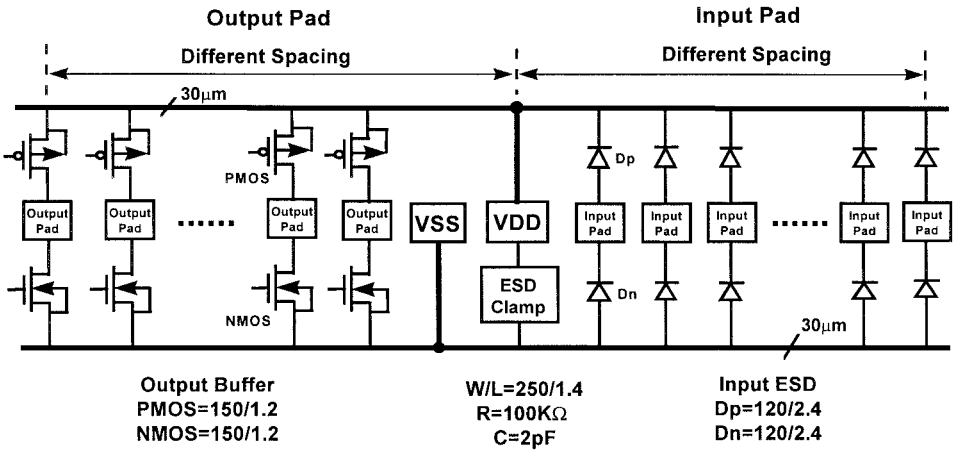



Fig. 14. Test chip design to investigate the pin-location spacing effect on the ESD-protection performance with the efficient VDD-to-VSS ESD clamp circuit.

stressed pad and the grounded pad in the IC. If the VDD-to-VSS ESD clamp circuit is located too far from the stressed pad and the grounded pad, as shown in Fig. 13, the speed and efficiency to bypass the ESD current through the VDD-to-VSS ESD clamp circuit is seriously delayed and degraded by the parasitic resistance and capacitance along the power lines. Some ESD current is still discharged through the internal circuits and causes some ESD damages on the internal circuits. So, the pins of the IC may have different ESD levels, even if the pins have the same ESD protection circuits. The stressed pin has a higher ESD level if the stressed pin is closer to the VDD-to-VSS ESD clamp circuit. Therefore, a special design rule to specify the spacing from the input or output pins to the VDD-to-VSS ESD clamp circuit for effective whole-chip ESD protection has to be established.

An experimental test chip has been designed to investigate the pin-location spacing effect on the ESD-protection performance with the efficient VDD-to-VSS ESD clamp circuit. A schematic diagram of the experimental test chip to investigate the spacing effect is shown in Fig. 14. The VDD-to-VSS ESD clamp circuit is located on the VDD pad in the center of Fig. 14 and a VSS pad is adjacent to this VDD pad. The output pads are located at the left-hand part of Fig. 14 with different spacings to the VDD-to-VSS ESD clamp circuit. At each output pad, the output PMOS and NMOS devices have the same device dimension ($W/L$) of 150/1.2 ($\mu$m). The input pads are located at the right-hand part of Fig. 14 with different spacings to the VDD-to-VSS ESD clamp circuit. At each input pad, the diodes $D_p$ and $D_n$ have the same anode perimeter of 120 $\mu$m, and the spacing between the anode and cathode of the diodes is 2.4 $\mu$m. The device dimension ($W/L$) of the discharging NMOS used in the VDD-to-VSS ESD clamp circuit is 250/1.4 ($\mu$m). The resistor $R$ is about 100 k$\Omega$ and the capacitor C is about 2 pF in the VDD-to-VSS ESD clamp circuit to provide a $RC$ time constant of 0.2 $\mu$s. The metal width of both VDD and VSS power lines is drawn as 30 $\mu$m to investigate the spacing effect on the efficiency of ESD protection with the efficient VDD-to-VSS ESD clamp circuit.

This test chip has been fabricated in a 0.8-$\mu$m CMOS technology with LDD process. The HBM ESD testing results are measured in Figs. 15 and 16 to verify the spacing effect on the ESD-protection efficiency. In the HBM ESD test, the ESD pulse is applied to the stressed pin with three zaps per stress voltage level [12]. After the ESD stress, the test chip is inspected by the full function test including the leakage currents on the input, output, and VDD pins to judge whether the test chip is damaged by the applied ESD pulse. In Fig. 15(a), it shows the dependence of the input PS-mode

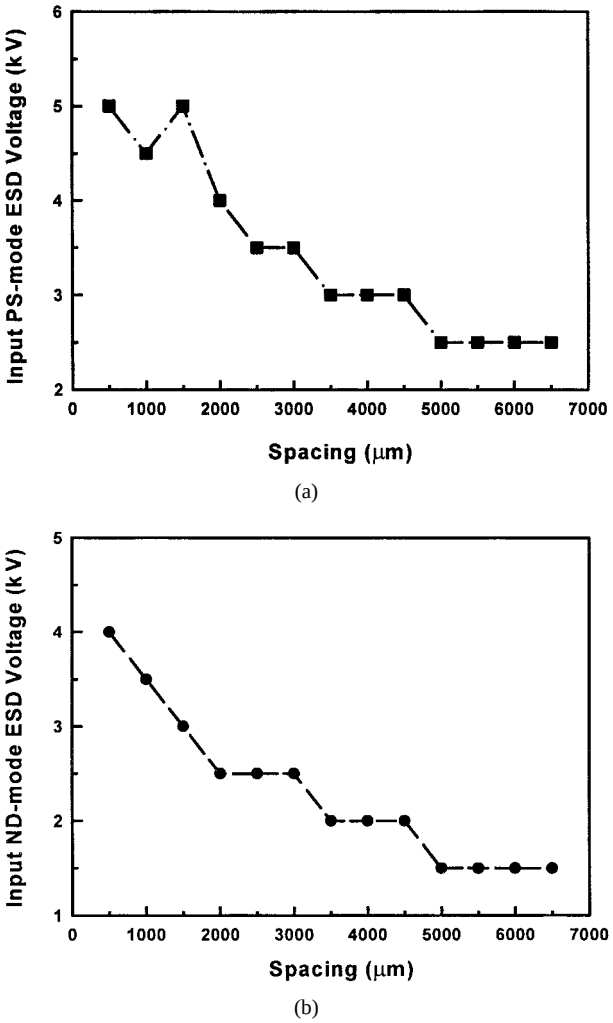



Fig. 15. Experimental results to verify the spacing effect on the HBM ESD robustness of the input pin in (a) the PS-mode and (b) the ND-mode, ESD-stress conditions.

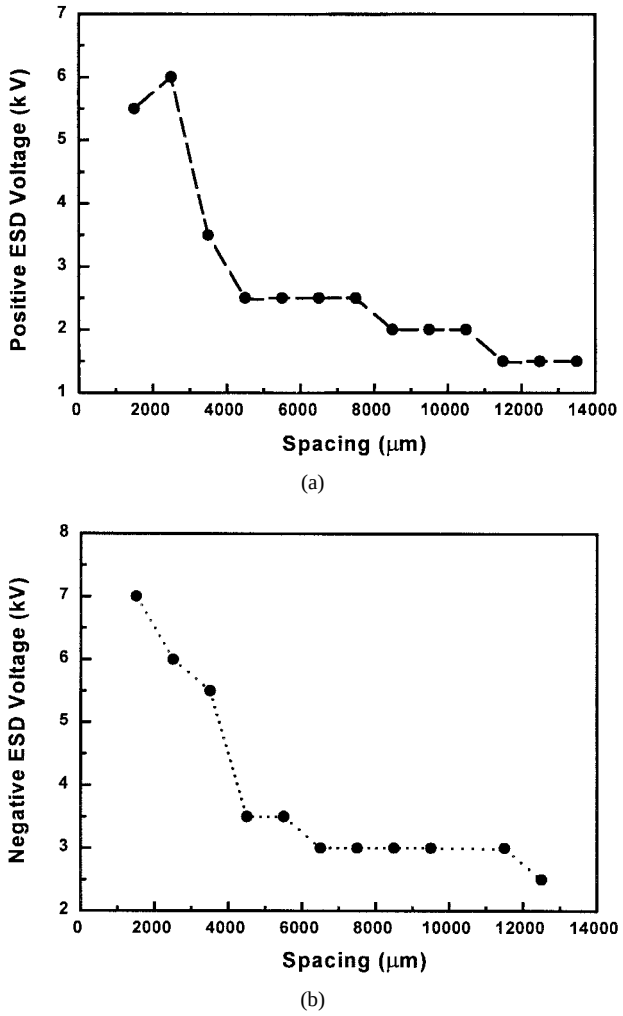



Fig. 16. Experimental results of the spacing effect on the HBM ESD robustness of the pin-to-pin ESD reliability from an ESD-stressed input pin to another relatively grounded output pin. (a) A positive ESD voltage and (b) a negative ESD voltage is applied to an input pin while another output pin is grounded, but other pins including the VDD and VSS pins are all floating.

ESD level on the spacing from the input pad to the VDD-to-VSS ESD clamp circuit. The ESD level of the input pad is significantly increased when the input pad is closer to the VDD-to-VSS ESD clamp circuit. The PS-mode ESD level of the input pad is improved from the original level about 2.5 kV to more than 4 kV, while the location spacing from the input pad to the ESD clamp circuit is below 2000 $\mu$m. In Fig. 15(b), it shows the dependence of the input ND-mode ESD level on the spacing from the input pad to the VDD-to-VSS ESD clamp circuit. The ND-mode ESD level of the input pad is improved from the original level about 1.5 kV to more than 3 kV, while the location spacing from the input pad to the ESD clamp circuit is below 1500 $\mu$m. The shorter distance from the input pad to the VDD-to-VSS ESD clamp circuit leads to a much higher ESD level of the input pad. This provides a new ESD protection concept to improve ESD level of the input pin by only using the efficient VDD-to-VSS ESD clamp circuit but without increasing the device dimensions in the input ESD protection circuits.

The pin-to-pin ESD protection performance is measured in Fig. 16(a) and (b). In Fig. 16(a) and (b), a positive (negative) ESD voltage is applied to some input pin of Fig. 14, while another output pin is grounded but the other pins including the VDD and VSS pins are all floating, to investigate the spacing effect on the pin-to-pin ESD protection with the efficient VDD-to-VSS ESD clamp circuit. In Fig. 16(a), the positive pin-to-pin ESD level is increased greater than 3.5 kV while the spacing between the stressed input pad and the grounded output pad is less than 3000 $\mu$m. In Fig. 16(b), the negative pin-to-pin ESD level (in magnitude) is increased greater than 5.5 kV while the spacing between the stressed input pad and the grounded output pad is less than 3000 $\mu$m. By using the efficient VDD-to-VSS ESD clamp circuit, the pin-to-pin ESD level can be significantly improved if the spacing between the stressed pin and the grounded pin is not too large. To provide a 3-kV pin-to-pin ESD reliability for the CMOS IC with the power line width of 30 $\mu$m in the 0.8-$\mu$m CMOS process, the VDD-to-VSS ESD clamp circuit has to be repeatedly inserted between the VDD and VSS power lines in every distance of 3000 $\mu$m. The larger device dimension of the ESD-clamping NMOS in the VDD-to-VSS ESD clamp circuit, the wider metal width of the VDD and VSS power lines

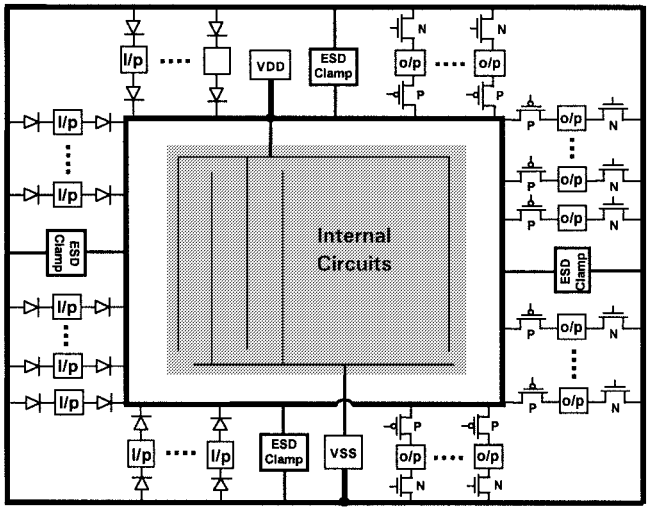



Fig. 17. Schematic diagram to show the concept of whole-chip ESD protection design with four efficient ESD clamp circuits between the VDD and VSS power lines in an CMOS chip.

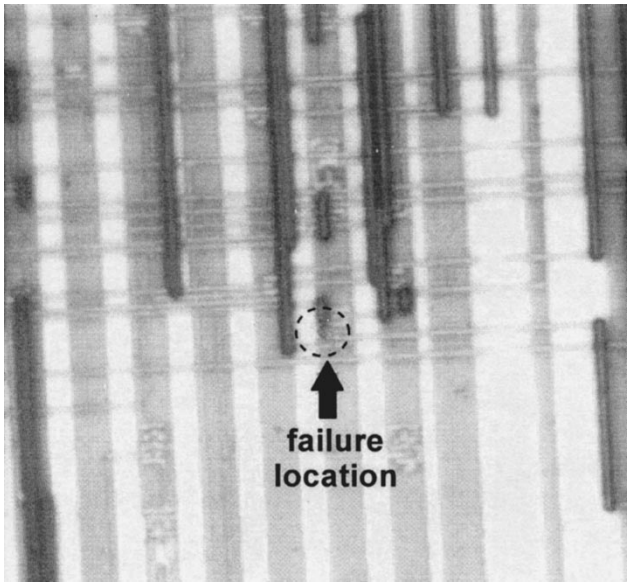



Fig. 18. Typical EMMI picture to show the failure location of ESD damage (indicated by the arrow) on the internal circuits due to pin-to-pin ESD stress.

surrounding the whole chip, and the shorter distance of every repeat of the VDD-to-VSS ESD clamp circuit can lead to a much higher pin-to-pin ESD protection. Through the detailed analysis and experimental investigation, a special ESD design rule for whole-chip ESD protection with efficient VDD-to-VSS ESD clamp circuits has been established in a 0.8-$\mu$m CMOS technology.

## IV. Application

The design concept of whole-chip ESD protection with efficient VDD-to-VSS ESD clamp circuits is illustrated in Fig. 17 to provide a real whole-chip ESD protection without the unexpected ESD damage in the internal circuits under any ESD-stress condition. Four VDD-to-VSS ESD clamp circuits are inserted in the four sides of the chip with the VDD and VSS power lines surrounding the whole chip. For a larger die size with a much longer VDD and VSS power lines, the numbers of the VDD-to-VSS ESD clamp circuits inserted between the power lines of the chip should be increased. The VDD-to-VSS ESD clamp circuits can be also placed in the four comers of the chip without increasing the total layout area of the chip. The comers are often empty without any device in the most IC's.

This whole-chip ESD protection design has been practically used to improve the ESD reliability of a 0.8-$\mu$m CMOS IC product. In the original ESD design of this IC product, two gate-grounded NMOS's ($W/L = 250/2$ for each NMOS, as illustrated in Fig. 5) are used as the VDD-to-VSS ESD clamp devices in the chip and placed around the VDD and VSS pads. The input and output ESD protection circuits are the same as those shown in Fig. 14. But, the ND- and PS-mode HBM ESD levels of the input and output pins of this IC are only around 1–1.5 kV, whereas the pin-to-pin HBM ESD level of this IC is only about 0.5–1 kV. The failure criteria to judge the ESD level of the IC includes the whole-chip function test and the leakage currents at all the input, output, and VDD pins. This ESD level is much below the minimum ESD specification of 2 kV in the commercial IC's, even if there are two gate-grounded NMOS's as the ESD-clamping devices between the VDD and VSS power lines. After the pin-to-pin HBM ESD stress, the failed IC has been processed to find the failure location. The EMMI (photon emission microscope) picture in Fig. 18 has shown that the ESD damage, indicated by the arrow, is located at the internal circuits beyond the input, output, and VDD-to-VSS ESD protection circuits. This has confirmed that the VDD-to-VSS ESD clamp circuit with the gate-grounded NMOS can not effectively protect the internal circuits in submicron CMOS technology, especially in the pin-to-pin ESD-stress condition.

To rescue the ESD level of this IC product, the proposed VDD-to-VSS ESD clamp circuits are inserted into the IC to perform the whole-chip protection without increasing the total chip size. The microphotography of this ESD-rescued IC product is shown in Fig. 19. Five efficient VDD-to-VSS ESD clamp circuits are added between the VDD and VSS power lines which are indicated by the five arrows in Fig. 19. One is inserted on the VDD pad and the others are inserted between the power lines at the left- and right-hand sides of the chip, whereas the input and output ESD protection circuits are kept the same in the IC product without any change. To achieve the whole-chip ESD protection design, the added five efficient VDD-to-VSS ESD clamp circuits have to be uniformly placed in the chip as that suggested in Fig. 17. By using this proposed whole-chip ESD protection design without increasing the total chip size, the ND- and PS-mode ESD levels of this IC product has been improved to above 4 kV and the pin-to-pin ESD level is also improved to above 3 kV, which is much greater than the commercial ESD specification of 2 kV. The pin-to-pin ESD level is guaranteed by full function verification after the IC is stressed under any ESD testing condition of Fig. 2. After the pin-to-pin ESD test, the failed IC is also processed to find the failure location. The failure is located on the VDD-to-VSS ESD-clamping NMOS and causes a leakage current in the order of mA from VDD to VSS power lines. The failure

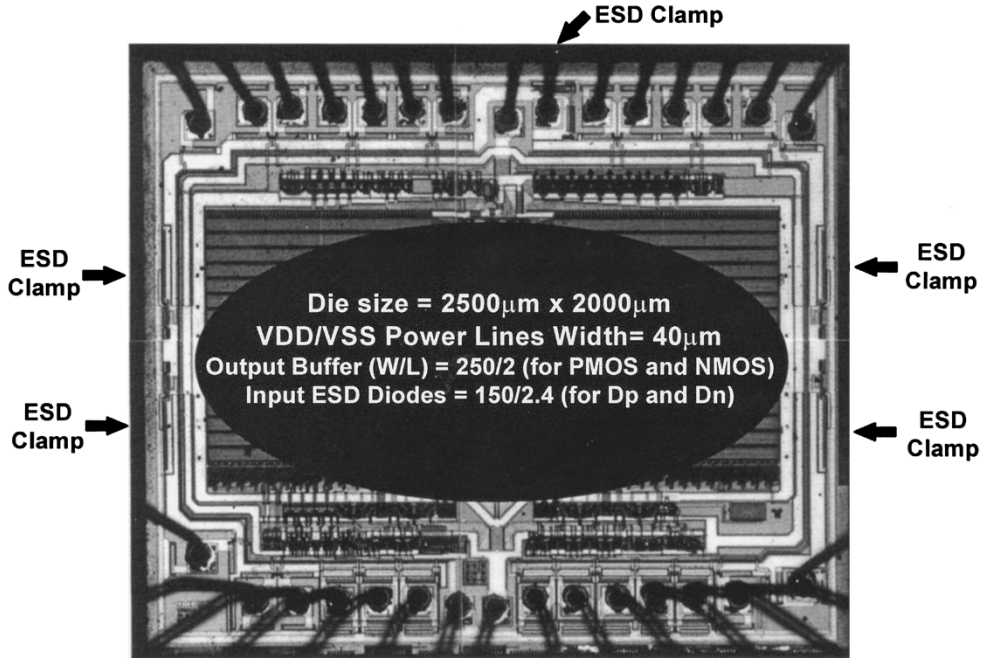



Fig. 19. Microphotograph of a 0.8-$\mu$m CMOS IC product using the proposed whole-chip ESD protection design with five VDD-to-VSS ESD clamp circuits (indicated by the arrows).

location is not found in the internal circuits of the failed IC. So, the internal circuits of this IC product can be fully protected against ESD damage by this proposed whole-chip ESD protection design with suitable spacing distribution to add the efficient VDD-to-VSS ESD clamp circuits into the chip.

## V. Conclusion

Based on the $RC$ time delay, an efficient VDD-to-VSS ESD clamp circuit has been designed to provide a low-impedance path between the VDD and VSS power lines to quickly bypass the ESD current during the ESD-stress condition. With the efficient ESD clamp circuit between the VDD and VSS power lines, the internal circuits of an IC can be really protected against ESD damage. However, due to the parasitic resistance and capacitance along the power lines, different pin location of the same input (or output) ESD protection circuit in an IC causes different ESD level. The pin has a much higher ESD level, if this pin is closer to the efficient VDD-to-VSS ESD clamp circuit. In order to investigate the pin location effect on the ESD protection, an experimental method has been demonstrated to find the ESD design rule for inserting the efficient VDD-to-VSS ESD clamp circuits. A whole-chip ESD protection design has been established by using multiple VDD-to-VSS ESD clamp circuits. The efficient VDD-to-VSS ESD clamp circuits are repeatedly inserted between the VDD and VSS power lines in every distance of 3000 $\mu$m to provide a 3-kV pin-to-pin HBM ESD level in a 0.8-$\mu$m CMOS process with the power line width of only 30 $\mu$m. Such a whole-chip ESD protection design has been successfully applied to rescue the ESD level of an IC product in a 0.8-$\mu$m CMOS technology. Without increasing the die size of the IC product, the ESD level of the input or output pins has been improved from the original 1 kV to above 4 kV. The pin-to-pin ESD level of the IC product has also improved from the original 0.5 kV to above 3 kV without causing any ESD damage in the internal circuits of the IC. This whole-chip ESD protection concept can be expanded to protect the IC's with multiple VDD or VSS power pins.

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