JEDEC STANDARD

Compact Thermal Model Overview

JESD15-1

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COMPACT THERMAL MODEL OVERVIEW DOCUMENT

(From JEDEC Board Ballot JCB-08-28, formulated under the cognizance of the JC-15.1 Committee on Thermal Characterization.)

1 Scope

This document should be used in conjunction with the master document, "Methodology for the Thermal Modeling of Component Packages[1]", the "Terms and Definitions document[2]", and subsidiary documents as they become available.

This document is intended to function as an OVERVIEW to support the effective use of Compact Thermal Model (CTM) methodologies as specified in the companion methods documents. At present, there are two such documents: "Two-Resistor Compact Thermal Model Guideline[3]" and "DELPHI Compact Thermal Model Guideline[4]."

The planned structure for this set of documents is indicated in Figure 1.

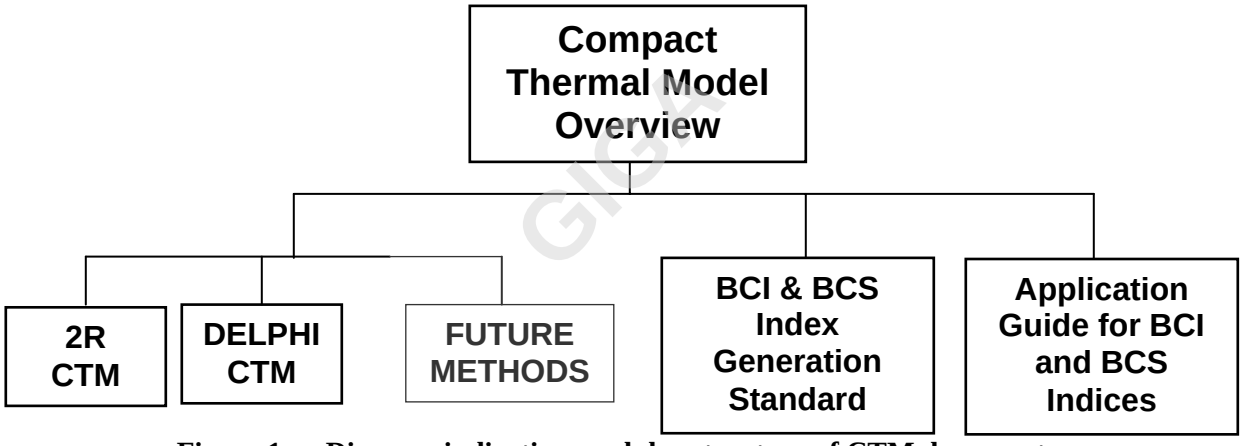

Figure 1 — Diagram indicating modular structure of CTM documents

This OVERVIEW is intended to provide a context for the comparison of CTM methods by defining a number of qualitative criteria. A procedure for quantifying the relative accuracy of different CTM methods by the calculation of Boundary Condition Independence (BCI) and Boundary Condition Subset (BCS) Indices will be specified in the future document, BCI & BCS INDEX GENERATION STANDARD. The APPLICATION GUIDE FOR BCI AND BCS INDICES will be added at a later date to support the effective use of these indices.

In the realization that CTM methodology will continue to evolve, this modular structure has been adopted for the generation of appropriate standards and guidelines. The intent is that, as a CTM method reaches a certain level of maturity and recognition in the industry, a standard or guideline governing its use would be added as a subdocument to this OVERVIEW.

2 Normative references

The following standards contain provisions that, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below.

1. JESD15, *Methodology for the Thermal Modeling of Component Packages,* 2008.

2. JESD15-2, *Terms and Definitions for Modeling Standards.*

3. JESD15-3, *Two-Resistor Compact Thermal Model Guideline,* 2008

4. JESD15-4, *DELPHI Compact Thermal Model Guideline,* 2008

5. JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions — Junction-to-Board,* Oct. 1999.

6. JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information,* May 2005.

3 Background

Thermal simulation has grown in importance as a method of characterizing the thermal behavior of electronic systems. The technology of thermal simulation has matured to the point that it is possible to represent the system construction and circuit board layout in considerable detail, down to the component level.

However, at the present time, the components themselves are often represented with a considerably simplified geometry due to computational limitations. To deal with this issue, it is common practice to create individual detailed submodels of the various semiconductor packages and other components in this system. Using the submodel results, it is then possible to create a simplified model of the component which accurately represents its thermal performance when inserted into the system-level simulation.

Unfortunately, there are many barriers to executing this modeling strategy in an efficient manner. Frequently the engineer performing the system-level model lacks the detailed information required to construct accurate component-level submodels. Furthermore, the necessity for the construction of component-level submodels adversely impacts the time to complete the system-level analysis.

It is a more efficient allocation of effort for component suppliers to perform the thermal characterization of their own products. The supplier is best positioned to understand the construction of their products and to validate the accuracy of component-level models. Furthermore, the supplier has a vested interest in seeing to it that the thermal performance of their products corresponds to that represented by any models released to their customers.

3 Background (cont'd)

Finally, the interests of the component supplier are protected in that they can control the accuracy of the component-level model. If the model is performed at the user site, the component supplier will usually have no control over the accuracy of the analysis.

A Compact Thermal Model (CTM) as defined by this document represents a special class of *simplified component models* which satisfy the technical requirements of accuracy and software compatibility and also act as a viable means of exchanging the required data from supplier to customer in the world-wide electronics industry.

4 Vision statement

A CTM is a simplified component model intended to reproduce the thermal behavior of a component in a wide variety of system-level simulations. Its ultimate purpose is to allow a component-level thermal model generated at the component supplier to be efficiently inserted in a system-level thermal simulation conducted within another organization. As such, it should satisfy certain criteria as detailed below.

5 Properties of a compact thermal model

A CTM as defined herein should have the following properties.

- It should be of limited complexity. In today's technology, this equates to tens of nodes. It is conceivable that this number could increase over time with improvements in computer calculating power and the sophistication of CTM techniques.
- It should satisfy appropriate levels of Boundary Condition Independence (BCI). Absolute BCI is a property of a CTM whereby it calculates a chip temperature in all possible application environments, which is in perfect agreement with the results of a detailed model calculation. These environments, in essence, impose different boundary conditions on the component. It is a goal of the CTM standardization effort that CTMs should demonstrate a high level of BCI.
- It should be vendor- and software-neutral.
- A CTM generation technique should be adaptable to mainstream conduction codes for performing a package-level thermal analysis.
- The CTM should be capable of insertion into standard numerical codes for system-level (including board-level) analysis.
- It should be fully documented and nonproprietary.

6 History of compact thermal models

The methodology of representing the thermal behavior of microelectronic packages by resistor networks has been in existence for several decades. However, both the coining of the term Compact Thermal Model and the effort to establish standard methods of usage and data transfer began with the DELPHI project.

DELPHI (which stands for DEvelopment of Libraries of PHysical models for an Integrated design environment) was a project supported by a grant from the Esprit III technology development program of the European Community during the years 1993 – 1996 (project no. 9197). Under the auspices of this project, considerable work was performed to refine both the numerical and validation aspects of the CTM methodology. The work of the DELPHI project was extensively published. By the requirements of the grant, its work was required to lie in the public domain.

The CTM methodology was further developed during subsequent projects entitled SEED (Supplier Evaluation and Exploitation of DELPHI; Esprit III project no. 22797; 1997-1998) and PROFIT (Prediction of Temperature Gradients Influencing the Quality of Electronic Products; European Community IST Program, project no. 12529; 2000 – 2002). The CTM work was released into the public domain by means of reports and publications.

Members of the DELPHI, SEED, and PROFIT projects have continued to be active in the JC15 committee to promote an awareness of developments in CTM methodology and to participate in standardization efforts.

The JEDEC activities have emphasized enhancing the practical application of the DELPHI methods and, as much as possible, leveraging the existing JEDEC thermal standards to facilitate the adoption of these methods by the electronics industry, world-wide.

7 Criteria for comparison of CTM methods

A number of criteria have been established in order to provide a context for the comparison of CTM methods. They will be applied in this document to CTM methods defined by subsidiary documents.

- Is the CTM test based or simulation based?
  - A model may be extracted directly from test results or from simulations that, themselves, have been validated with test results.
- Does the CTM contain an artifact of the test environment?
  - A model extracted directly from test results may have embedded in it the contribution of different heat flow paths and the resultant temperature differences caused by the test fixturing and test environment. In general, CTMs that contain an artifact of the test environment will have lower accuracy than those that do not.

7 Criteria for comparison of CTM methods (cont'd)

- Does the CTM generation methodology inherently include an error analysis?
  - Simulation-based methods typically include this as a by-product of the optimization procedure to determine the best-fit values of the resistors in the CTM network. Methods that assign values to the resistors in a CTM directly from experimental measurements do not include an error analysis of the CTM as an integral part of the process of generating the resistor values.
- Calculation of BCI and BCS Indices.
  - A method of calculating a BCI Index will be specified in a future document. (This document is indicated in the roadmap as, "BCI & BCS INDEX GENERATION STANDARD.") It is intended to be a figure of merit indicating the level of boundary condition independence of CTMs generated using a particular method for a representative set of IC packages. It is intended to provide a common basis of comparison of the accuracy of alternative methods, including those without an inherent error analysis.
  - A second index is defined: the Boundary Condition Subset (BCS) Index. Its method of calculation will be specified in a future document. (This document is indicated in the roadmap as, "BCI & BCS INDEX GENERATION STANDARD.") However, it differs from the BCI Index in that the set of boundary conditions assumed in the calculation of each BCS Index corresponds to those encountered in specific application environments.
  - The comparison of values of BCI and BCS Indices for the methods described in the CTM series of documents will be presented in a future document. (This document is indicated in the roadmap as, "APPLICATION GUIDE FOR BCI AND BCS INDICES.")

8 BCI and BCS Indices

The specification of the BCS Index is intended to provide guidance to users of CTMs during the period of transition for CTM methods based on existing JEDEC test standards to those based on more advanced methods, such as the DELPHI method. Methods based on current JEDEC test standards are expected to provide reasonable accuracy for applications resembling the test conditions, but reduced accuracy for others. The BCS Index is intended to make clear to the end user the level of accuracy such CTMs can achieve for a specific application.

The supplier of a CTM is requested to disclose calculated values of BCI and BCS Indices as is appropriate to provide the end user with adequate guidance regarding the accuracy of the CTM. If a method has a small BCI Index, indicating high accuracy over a wide range of boundary conditions, then it should not be necessary to provide values of the individual BCS Indices. However where this is not true, the supplier is requested, at minimum, to provide values of BCS Indices for the intended applications of the package. It would be beneficial to the user for the supplier to provide the BCI Index as well.

9 CTM methods

The CTM Methods defined to date incorporate several assumptions:

1) The package contains a single integrated circuit whose temperature is represented by a single temperature node.
2) The package is mounted to a printed circuit board (PCB).
3) Heat flows from the chip to:
   a. The package top surface. It then flows into the ambient fluid or to a heat sink attached to the top of the package;
   b. The side surfaces of the package. It then is transmitted into the ambient fluid.
   c. The package bottom surface and leads. It then flows into the PCB.
4) Thermal resistor networks are used to represent the heat flow paths.
5) Each external surface of the part may be considered to be at a single temperature represented by one node. Alternatively, the external surfaces can be subdivided into regions each with a single temperature corresponding to one node.

The CTM methods defined by JEDEC are the Two-Resistor Model and the DELPHI Model. They are described below.

9.1 Two-Resistor CTM

The Two-Resistor CTM represents the heat flow paths described in 3a and 3c (above) in the simplest possible way, namely using a single thermal resistor for each. This is illustrated in Figure 2. *Note that for the two resistor model, the heat path described in 3b is ignored.*

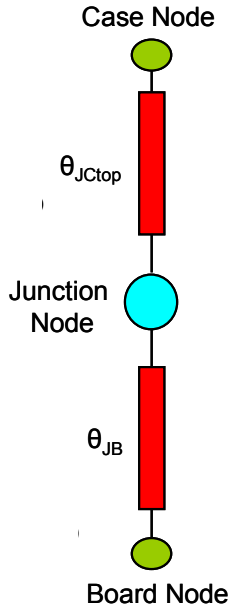

Figure 2 — Two-Resistor Model Network Topology

9 CTM methods (cont'd)

9.1 Two-Resistor CTM (cont'd)

The Two-Resistor Model consists of three nodes as depicted in the Figure 2. These are connected together by two thermal resistors, being the measured values of the Junction-to-Board[5] and Junction-to-Case[6] resistances described above.

NOTE JESD51-12 defines the use of the Junction-to-Case resistance. It does not define the test method to measure this quantity. The appropriate test method will be specified in a future document.

The heating power is applied at the Junction node.

The Board node is considered to be in direct thermal contact with the local environment immediately below the footprint of the package (normally the PCB).

The Case node is considered to be in direct thermal contact with the local environment immediately above the top of the package (normally air or a thermal interface material used in conjunction with a heat sink).

Thus there are only two paths for the heat to leave the Junction node and flow into the environment - through the Case node and through the Board node. No heat flow through the sides of the package is accounted for.

9.2 Application of standard CTM criteria to Two-Resistor Model

The Two-Resistor model has the following characteristics when rated according to the CTM criteria of Section 7:

- Is the CTM test-based or simulation-based?
  - The two resistors are extracted from JEDEC-standard thermal tests or a validated detailed thermal model that simulates the test environment.
- Does the CTM contain an artifact of the test environment?
  - The junction-to-board resistor contains a contribution due to heat flow through the test board.
- Does the CTM generation methodology inherently include an error analysis?
  - The two-resistor CTM methodology does not contain an error analysis.
- Calculation of BCI and BCS Indices.
  - Will be specified in a future document.

9 CTM methods (cont'd)

9.3 DELPHI CTM

A DELPHI compact model is a thermal resistance network.

The DELPHI network is comprised of a limited number of nodes connected to each other by thermal resistors or links. A possible configuration is shown in Figure 3. In effect, the complex 3D heat flow within a real package is represented by a series of links.

Network nodes are, by definition, each associated with a single temperature only. They can be either surface or internal.

- Surface nodes are associated with a physical region of the package surface defining the area of the node. In such a case, the nodal temperature represents the average temperature of the area allocated to the node in the actual package. Internal nodes lie within the package body and may or may not correspond to a physical region within the package. Surface nodes must always have a direct one-to-one association with the corresponding physical areas on the actual package. Therefore, it is critical that they communicate with the environment in the same manner as the package surfaces they represent.
- Surface nodes communicate with internal nodes as well as the surrounding environment.
- Internal nodes do not communicate with the environment directly; however they may have a heat source associated with them (for example, to represent the heat flow from a die within the package).

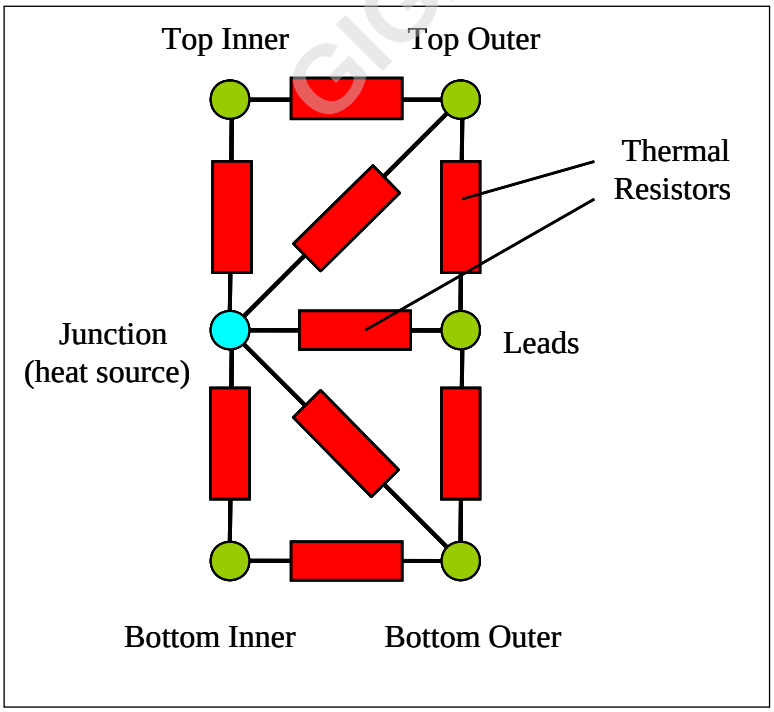

Figure 3 — Example of a Compact Model Network Topology

9 CTM methods (cont'd)

9.4 Application of standard CTM criteria to DELPHI model

The DELPHI model has the following characteristics when rated according to the CTM criteria in 7:

- Is the CTM test-based or simulation-based?
  - It is simulation-based. The values of the resistors in the network topology representing the package are chosen by minimization of the Objective Function.
- Does the CTM contain an artifact of the test environment?
  - The network representing the package does not contain any resistors representing heat flow in the test board. Thus, the DELPHI model contains no artifact of the test environment.
- Does the CTM generation methodology inherently include an error analysis?
  - The statistical procedure used to extract optimum values for the individual resistors inherently includes an error analysis.
- Calculation of BCI and BCS Indices.
  - Will be specified in a future document.

10 Bibliography

Selected published documents related to CTM history and methodology.

1. W. Krueger and A. Bar-Cohen, "Thermal characterization of a PLCC-expanded R_{jc} methodology" *IEEE Transactions on Components and Packaging Technologies,* Vol. 15, 1992, pp. 691-698.

2. H. Rosten, C. Lasance, and J. Parry, "The World of Thermal Characterization According to DELPHI – Part I: Background to DELPHI," *IEEE Transactions on Components and Packaging Technologies,* Vol. 20, 1997, pp. 384-391.

3. C. Lasance, D. den Hertog, and P. Stehouwer, "Creation and Evaluation of Compact Models for Thermal Characterization Using Dedicated Optimisation Software," *Proceedings of the Fifteenth IEEE SEMI-THERM Symposium*, 1999, pp. 189-200.

4. Aranyosi, A. Ortega, J. Evans, T. Tarter, J. Pursel, and J. Radhakrishnan, "Development of Compact Thermal Models for Advanced Electronic Packaging: Methodology and Experimental Validation for a Single-Chip CPGA Package," *Proceedings of the ITHERM Conference*, 2000, pp. 225-232.

5. E.G.T. Bosch, "Thermal Compact Models: An Alternative Approach," *IEEE Transactions on Components and Packaging Technologies,* Vol. 26, 2003, pp.173-178.

6. H. Pape and G. Noebauer, "Thermal Characterization of Active Components," *Electronics Cooling,* Vol. 4, No. 2, 1999, pp. 38-43.

10 Bibliography (cont'd)

7. H. Pape, and G. Noebauer, "Generation and Verification of Boundary Independent Compact Thermal Models for Active Components According to the DELPHI/SEED Methods," *Proceedings of the Fifteenth IEEE SEMI-THERM Symposium*, 1999, pp.201-211.

8. M. Rencz, V. Szekely, and E. Kollar, "Measuring Dynamic Thermal Multiport Parameters of IC Packages", *Proceedings of the 6th THERMINIC Workshop*, Budapest, 2000, pp.244-249.

9. C. Lasance, "Recent Progress in Compact Thermal Models," *Proceedings of the Twenty-first IEEE SEMI-THERM Symposium*, San Jose, CA, 2003, pp. 290-299.

10. C. Lasance, "The Influence of Various Common Assumptions on the Boundary-Condition-Independence of Compact Thermal Models," *IEEE Transactions on Components and Packaging Technologies*, Vol. 27, 2004, pp.523-529.

11. H. Pape, D. Schweitzer, J. Janssen, A. Morelli, C. Villa, "Thermal Transient Modeling and Experimental Validation in the European Project PROFIT," *IEEE Transactions on Components and Packaging Technologies*, Vol. 27, 2004, pp.530-539.

12. M.-N. Sabry, "Higher-Order Compact Thermal Models," *Proceedings of the 10th THERMINIC Workshop*, Sophia-Antipolis, 2004, pp.273-281.

13. M.-N. Sabry, "Compact Thermal Models for Electronic Systems, "*IEEE Transactions on Components and Packaging Technologies*, Vol. 26, No. 2, 2003, pp.179-185.

14. M.-N. Sabry, "Flexible- Profile Compact Thermal Models,"*Proceedings of 11th THERMINIC Workshop*, Belgirate, Italy, 2005, pp. 32-37.

15. M.-N. Sabry, "Dynamic Compact Thermal Models Used for Electronic Design: A Review of Recent Progress," *Interpack '03*, Paper No. 35185, Maui, July 6-11, 2003.

16. M-N. Sabry, S. Hossam, "Compact Thermal Models: A Global Approach," *Proceedings of 1st Theta Workshop*, Cairo, 2007, pp. 51-57.

17. C. Lasance, "Ten Years of Boundary-Condition-Independent Compact Thermal Modeling of Electronic Parts: A Review," Heat Transfer Engineering, Vol. 29, Issue 2, 2008, pp.149-168.

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