Application of Thermal Network Approach to Electrical-Thermal Co-simulation and Chip-Package-Board Extraction

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Abstract

Today's electronic products are getting highly integrated. The thermal design can no longer be separated from the electrical design, and the chip, package and PCB (Printed Circuit Board) designs are tightening in the system design process. To address this challenge, the system level electrical-thermal co-design and optimization are of importance. In this paper, two different numerical approaches are presented on the system level electrical-thermal co-simulation of Huawei's computer server. The first one is based on the detailed modeling of chips, package and PCB, and the traditional finite element method (FEM) is used for the co-simulation. It has its accuracy advantage, and can provide detailed assessments of the system's electrical and thermal performances, and also the couplings between them. This approach is demonstrated through an electrical-thermal co-simulation of a merged chip, package and PCB design in the server. The second approach is based on a novel dynamic thermal model which has demonstrated high accuracy and efficiency especially in transient analysis of a complex system, and the fast network simulator is used for the system-level thermal simulation. In this paper, the computer server is decoupled into multiple domains such as air flows, chassis, heat sinks, PCB boards, packages, etc., and the thermal system can be reconstructed as an integrated model-based network. Both steady and transient thermal simulations are presented, and thermal simulation results are validated with the experimental data.

Keywords

System level, electrical-thermal, dynamic thermal model

1. Introduction

As electronic integration density continuously grows, voltage and temperature control has become increasingly stringent. In consideration of reliability assessment, components require precise control of temperature at each via/ball/bump/pin [1-2]. On the other hand, the increasing current (up to Hundreds of Ampere) of power delivery could also bring reliability concerns; it is inevitable to take thermal effects into account since Joule heating cannot be ignored in high current cases [3]. Analysis without considering the electrical and thermal interaction will definitely lead to inappropriate voltage, current and temperature evaluation. Consequently, the Joule heating generated by the current loss on conductors in the electrical simulation needs to be taken into account in the thermal analysis. At the same time, the temperature rise caused by the thermal simulation results in conductivity reduction of conductors should also be considered in the electrical analysis [3-4]. Therefore, electrical / thermal co-simulation is a proper way to meet actual design requirements.

Among various simulation methods, the finite element method (FEM) including advanced meshing technique is employed in the current study based on its proven accuracy and capabilities of handling complicated geometry [5]. In this paper, electrical/thermal co-simulation for merged layout of PCB/package/die with component power dissipation, Joule heating, heat sink and air convection are investigated. The goal is to study the interactions of electrical/thermal co-simulation, and get the simulation results which are closest to the actual application of products. Typical maximum tolerated temperature for silicon die of a high power server is usually 105°C. Without proper ambient conditions or heat sinks, the operating temperature of the die can easily exceed the maximum value. The ultimate goal of thermal management is to effectively dissipate the heat in the silicon die to the ambient. Hence the heat sink and forced convection fluid flow are strongly necessary [6-7]. A computational fluid dynamics (CFD) technique will be necessary to greatly improve simulation results [2]. Ultimately, the temperature distribution of the package and PCB will be experimentally measured by using thermocouple or infrared camera and then compared with the simulation results for closed loop verification. Moreover, power dissipation and temperature profiles in the package and PCB obtained from electrical/thermal co-simulation are available for judging the reliability of the passive components within PCB such as resistors, capacitors and inductors [8]. A summarized pass/fail results table of components can be achieved based on these temperature maps. It will be desirable to assign temperature dependent models for passive components in further SI/PI analysis of the system design.

Compact thermal models such as 2-resistor model and DELPHI model have been widely used for thermal analysis and is best known for its low computational cost. Recently, a network-based approach has been developed for thermal simulation of electronic systems [2]. This approach is based on a BCI (boundary condition independent) dynamic thermal model which makes it possible to decouple the modeling of solid and fluid regions and integrates them later on. The approach consists of four steps,

(1) Thermal model extraction: each electronic part in a system such as the PCB, package, etc., can be extracted separately to generate the model. The model generation is based on the detailed 3D design structure without any simplification, and FEM-based numerical algorithm is used for the extraction.

(2) Fluid extraction: it is performed by using traditional CFD approach to form the thermal resistances between fluid and solids.

(3) System network assembly: Once all sub-networks are generated from solid and fluid extractions, the system network is assembled together with the power inputs to form the integrated thermal network of the system.

(4) System thermal simulation: the traditional network fast solver is used for both steady state and transient thermal simulation. The temperature behaviors of thermal probing nodes in the system are computed and reported.

In essence, the network-based thermal model employs a divide-and-conquer approach for thermal modeling. The model size in a network-based approach significantly reduces due to the decoupling of solids and fluid modeling as well as the separation of solid parts. This makes it possible to efficiently solve a large thermal system. In comparison with the traditional CFD approach which typically ignores 3D design details, the simulation accuracy will be preserved by using the accurate thermal model.

2. FEM-based system-level electrical/thermal co-simulation

A 3D electrical/thermal co-simulation based on finite element method (FEM) is employed in the present study. Fig.1 illustrates the scheme and process of electrical/thermal co-simulation flow, where IR drop analysis due to direct current (DC) and thermal simulation are working together. In electrical simulation, the temperature rise generated by current density as Joule heat source will be put into the thermal simulation, in addition to the component heat sources. This flow is essential because the power dissipation and Joule heat will increase the component temperature and lead to conductivity deterioration in the conductors. It also affects the voltage and current distribution, which then will further influence the temperature distribution. The electrical and thermal analysis are interacting with each other repeatedly until they stably converge [1-2].

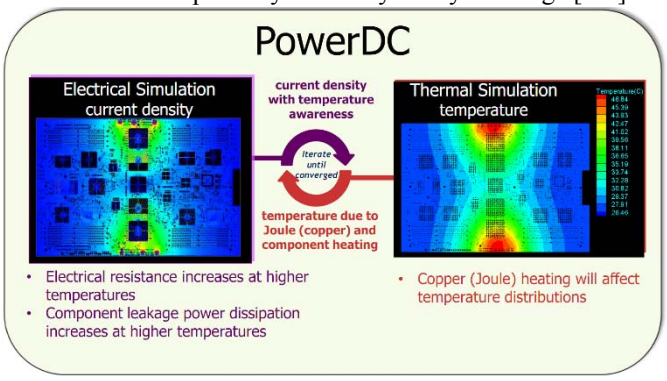


Figure 1. Electrical / thermal co-simulation flow

The numerical method of FEM is applied to solve electrical and thermal equations. The Joule heating often needs to be calculated at a particular location in space. The differential form of Joule heating equation gives the power per unit volume as below:

$$\frac{dP}{dV} = J \cdot E \tag{1}$$

Where, J is a vector indicating the current density, and E is a vector representing the electric field. The current flowing through interconnects obeys Ohm's Law:

$$J = \sigma E \tag{2}$$

Here, σ is the electrical conductivity depending on temperature. Therefore, the heat source includes both the component heating and Joule heating is:

$$\frac{dP}{dV} = J \cdot E = J \cdot \frac{J}{\sigma} = J^2/\sigma \tag{3}$$

The thermal simulation of heat transport is governed by

$$-\nabla \cdot \mathrm{K}\nabla \mathrm{T} = \frac{\partial}{\partial_x}\left(K_x \frac{\partial_T}{\partial_x}\right) + \frac{\partial}{\partial_y}\left(K_y \frac{\partial_T}{\partial_y}\right) + \frac{\partial}{\partial_z}\left(K_z \frac{\partial_T}{\partial_z}\right) = Q \tag{4}$$

Where T is temperature distribution, k is the thermal conductivity and Q is the heat sources including component heating and Joule heating. Simultaneously, the temperature-dependent conductivity σ can be expressed as:

$$\sigma_{T'} = \frac{\sigma_T}{1 + \alpha(T - T')} \tag{5}$$

Here σT′ is conductivity at temperature T′, σT is conductivity at temperature T and α is a temperature compensation coefficient of the material. The coupled co-simulation will solve the above equations by iteration, and the voltage/current distributions and thermal results at the equilibrium state will be obtained until convergence is reached.

3. Model-based system-level electrical/thermal co-simulation

The FEM method provides a very detailed and accurate solution for thermal systems. However, the simulation could be very time-consuming for large systems and greatly increase the design cycle time. Therefore, a model-based approach is introduced to simulate a complex thermal system.

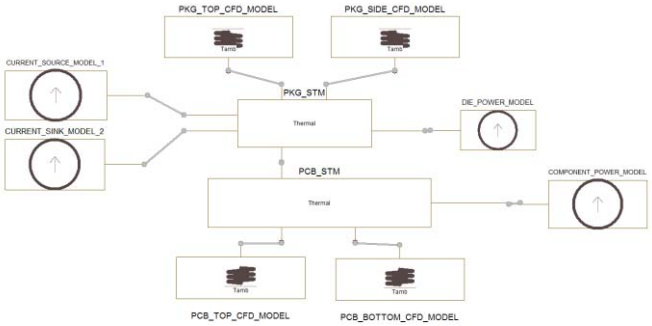


Figure 2. Model-based electrical / thermal co-simulation flow

In the flow, a thermal system is constructed by 4 types of models: solid thermal model, system CFD model, power model and current source model.

Here the thermal models are used for solid objects such as package and PCB board. The thermal models are extracted from the package and PCB design files, and various numerical methods including the FEM method and adaptive meshing are adopted in the thermal model generation. It has demonstrated distinct advantages like being a dynamic thermal model which can predict both the static and transient thermal behaviors of the electronic parts, and it also includes the Joule heating effect which makes the electrical/thermal co-simulation possible.

The CFD model consists of thermal resistances between solids and their environment and is extracted from the field solution of a CFD simulation. In the flow, a CFD simulation model will be directly generated from the chip-package-board FEM model, and the component and Joule heating effects will be activated in the CFD simulation model. All these

implementations will enhance the efficiency and accuracy of the CFD model extraction.

The power model provides the input power sources for the system. It could be a static, time-dependent or temperature-dependent power source. The temperature response and heat flow to the power input can be measured and monitored through the simulation results of the system.

The current source model describes the DC current value or profile applied to the system. And the Joule heating effect within the system can be enabled in the system-level electrical-thermal co-simulation. Temperature rise due to Joule heating will be taken into account in the overall system or at specific hot spots, which is of importance for the large current package designs.

4. Results

4.1 FEM-based electrical-thermal co-simulation

To demonstrate the first approach, a sixteen-layer PCB board merged with package and silicon die have been investigated in electrical/thermal co-simulation. Fig.3 shows a diagram of a layout of the PCB and PKG with an external heat sink. Here we focus on the main CPU core, where the fin heat sink has been proven to be the most fundamental method to dissipate heat to the ambient. A 83.13W heat source is placed on the silicon die within the PKG of the CPU core while the ambient temperature is set to be 28.9 ºC.

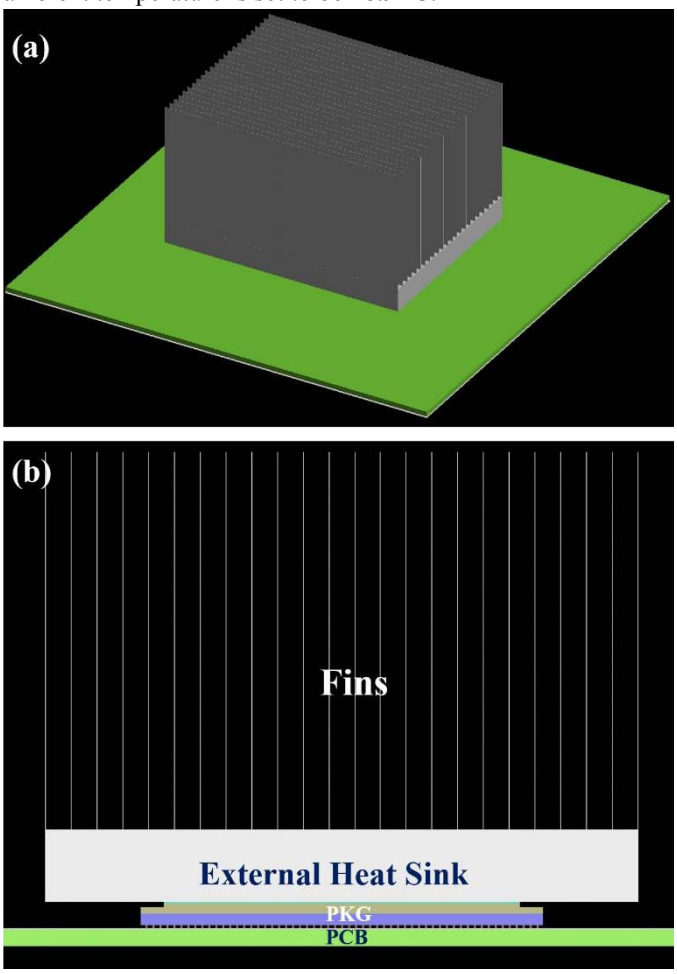


Figure 3 Top: Diagram of merged layout of PCB and PKG, 3D drawing; Bottom: Diagram of merged layout of PCB and PKG, with a side view of the package and PCB.

First, the thermal effects on electrical analysis are investigated in still air condition, where DC IR drop analysis and electrical/thermal co-simulation are performed respectively. As can be seen from Table 1, without Joule heating effect, the power loss for DC IR drop is 3.02W, among which 0.26W is from the PKG and the PCB board contributes 2.75W. However, with Joule heating under the same environment conditions, the power loss is up to 3.42W, with a 13.25% growth. The voltage drop with co-simulation is almost 6.02mV more than an electrical analysis. Similarly, compared with the electrical/thermal co-simulation analysis, the maximum temperature calculated from thermal only simulation is 76.46ºC, down 1.24 percent. Table 2 shows that Joule heating in this case has little contribution in terms of silicon die temperature and PCB board temperature in this situation. Nevertheless, when the power consumption increases to 190W in another case, the power loss comes up to 22W and the temperature difference can reach 6.5 º C. In view of high current and large power consumption trends in electronic designs, analysis without considering thermal and electrical coupling effects would most likely result in inaccurate assessments.

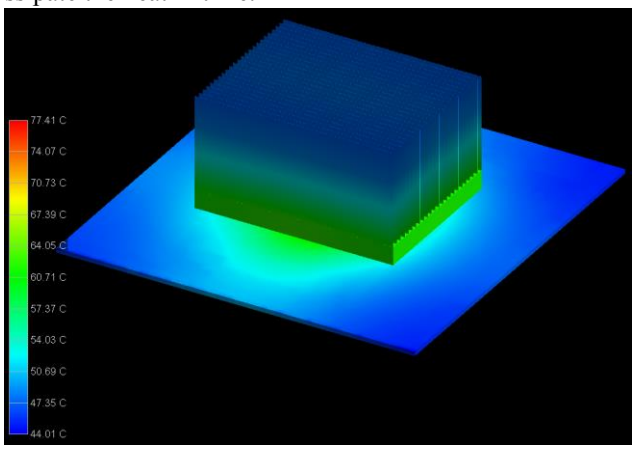
Table1: Electrical results comparison

Ambient 0m/s	Power Loss (W)			Voltage Drop (mV)		
	PCB	PKG	Total	Power	GND	Total
IR drop	2.75	0.26	3.02	54.90	7.96	62.86
Co-sim	3.11	0.31	3.42	60.07	8.81	68.88

Table2: Temperature results comparison

Maximum Temperature	Thermal only	Electrical/thermal co-simulation	Joule Heating
On die	76.46 ºC	77.42 ºC	0.96ºC
On PCB	73.71 ºC	74.92 ºC	1.21ºC

Another aspect we intend to explore is the reliability of the silicon die, which greatly depends upon the amount of time of application at high temperatures. For a very short period of time, a silicon die can tolerate temperatures well above the acceptable values. However, it becomes dangerous if time prolongs. Therefore, forced air cooling will be necessary since the maximum temperature of the silicon die is 77.41 ºC as shown in Fig. 4. It suggests natural convection is inadequate to dissipate the heat in time.



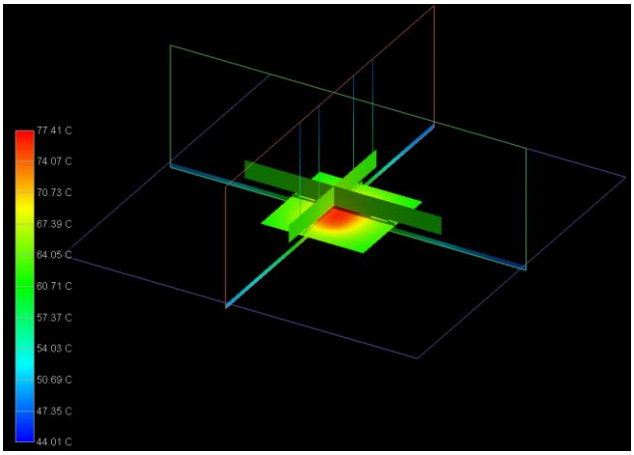


Figure 4 (a): Temperature distribution of co-simulation (b) Sectional views of the slice plane.

4.2 Experimental Setup and Measurements

In order to guarantee long lifetime for a computer server, the maximum temperature of ICs and other components inside the server must not be exceeded. To better understand the component's thermal performance, it is important to accurately measure the junction temperature at maximum operation of IC1.

Temperature measurement generally includes: contact thermometry and radiation thermometry. The former methodology commonly uses a thermo-couple which always remains in contact with the test device, while the latter thermometry adopts an infrared sensor to measure the radiation of the test device without contact. Here we use thermocouples with a temperature recorder to measure and record the corresponding temperature. As shown in the following figure, is a simplified diagram of the testing environment, including a computer, a temperature recorder with multi thermocouples, a chassis with four cooling fans and tested board. There are two processors on the motherboard and it also includes different components such as chipset DIMM sockets, power MOSFETs, daughter board, and some capacitors and inductors. The temperature measurement focuses on two positions, Probe1 is placed on the top side of IC1 package (just under the heat sink) and Probe2 is located on the PCB top near IC1. The test is performed at room temperature 25 °C. On the different positions, thermocouple ends are attached with the help of thermal grease.

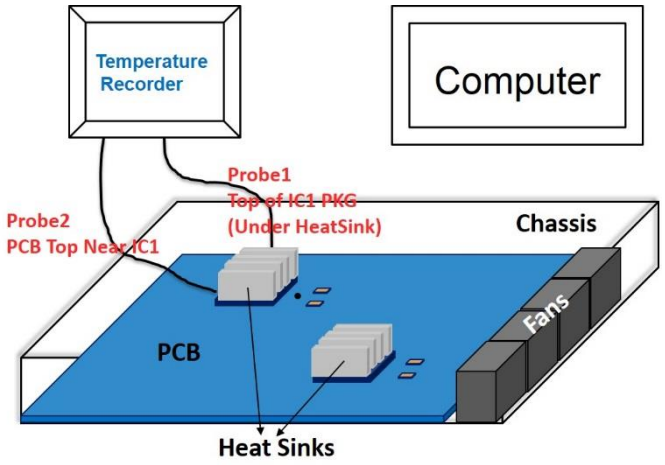


Figure 5 Simplified diagram of testing environment

In the current test scenario, only IC1 is in normal operation and the following Table 3 indicates the detail power specifications of the various components.

Table 3: Power information of components inside the server.

Components	Max-Power	Notes
IC1	82.4 / 77.8 / 64.5 /41.8/31W	Different status with different power
IC2	10W	Power On but without Service States
DIMM	10W	One DIMM works
MOS	1.3W	Per MOSFET
DB-U30	7.3W	Daughter Board
DB-U35	2.4W	Daughter Board

When the system is powered on, the four fans rotate at a high speed and forced air passes through the components on the board. The air speed is measured by a Fluke hot wire anemometer, and the measured air speed near the fans is almost 5m/s, note that the precision of anemometer is about 0.01m/s.

The following table shows the experimental measurements of two probes while the server is operating at partial or fully loaded conditions at steady state. Obviously, the measured temperatures constantly rise as the chip power consumption increases gradually. The temperature of the top side of IC1 package is almost 53°C when the power consumption reaches 82.4W.

Table 4: Measured temperature of different power dissipation.

Temp	P1-31W	P2-41.8W	P3-64.5W	P4-82.4W
Probe1	35.02 °C	39.10 °C	46.86 °C	53.00 °C
Probe2	30.60 °C	30.70 °C	34.55 °C	35.75 °C

Research on temperature transient response of the IC1 package during the measurement of different power consumption modes, is shown in the following figure:

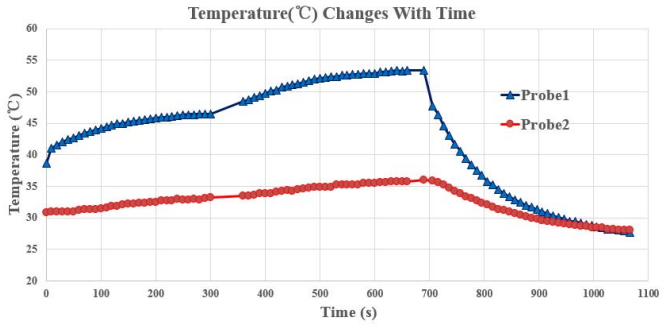


Figure 6 Measured surface temperature of Probe1 and Probe2 in different power consumption modes.

When the chip current changes from 28A to 51A within several seconds, the total chip power consumption increases extremely fast from 41.8W to 64.5W, as shown in the above figure. From 0 to 10 seconds, the temperature increased from 38.7 °C to 41 ° C, and then increased up to 46.4 ° C in 300 seconds. After one minute, the chip current changes from 51A to 71.25A, with a power consumption increase from 64.5W to 82W, the temperature rapidly increased to 48.7 ° C, and changes to about 53.4 ° C after another 5.5 minutes. Then, after a reset operation, the current and the temperature decrease rapidly; it takes 200 seconds to drop from 53.5 °C to 31 °C, and then the temperature decreases slowly.

Obviously, the temperature changes dramatically when the current or power suddenly changes loads. In the present test scenario, it seems like the 200 seconds after each jump is significant, and then the temperature changes slowly. This is helpful for evaluating the temperature changes in different current and power consumption modes. Future research will be focused on large current and high power scenarios to better understand the temperature variation.

4.3 CFD approach

The fluid extraction was performed based on traditional CFD approach. To compare test results, we set the same boundary and working conditions in the CFD simulation. For example, we made the output air speed of four fans as 5m/s and the ambient temperature to 25 ° C. In addition, the power consumption of each component is set according to Table 3. Fig.7 shows a diagram of CFD model.

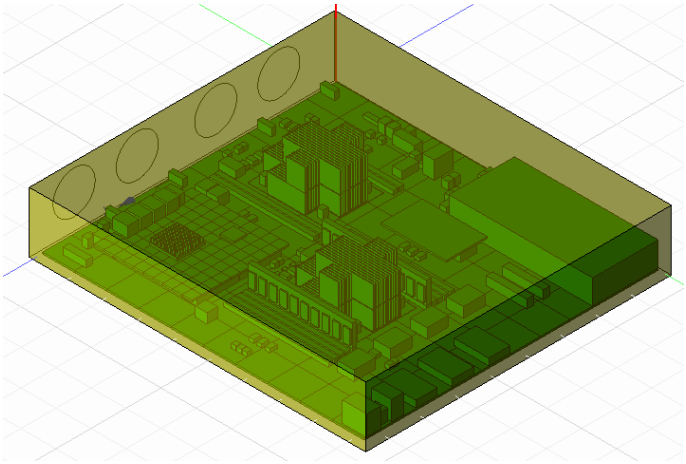


Figure 7 Schematic diagram of CFD Model

The steady-state temperature distribution results of CFD simulation under the maximum chip power consumption is shown in Fig.8, the temperature distribution result obtained by CFD deliver detailed information. For the IC1 die, the simulated temperature range is about 56.38 ˚C to 62.52 ˚C. Similarly, it is easy to determine the minimum and maximum temperatures of other devices or components, which gives an intuitive understanding of the temperature distribution in the whole system.

Table 5: Measured and CFD simulated temperature of different power dissipation.

Temp	P1-31W	P2-41.8W	P3-64.5W	P4-82.4W
Probe 1				
Probe1	35.02 °C	39.10 °C	46.86 °C	53.00 °C
CFD Simulator	35.05 °C	38.43 °C	45.52 °C	51.18 °C
△T_Probe1	**-0.03 °C**	**0.57 °C**	**1.34 °C**	**1.82 °C**
Probe 2				
Probe2	30.60 °C	30.70 °C	34.55 °C	35.75°C
CFD Simulator	29.96 °C	31.37 °C	34.35 °C	36.74 °C
△T_Probe2	**0.64 °C**	**-0.67 °C**	**0.20 °C**	**-0.99 °C**

Table 5 shows a comparison between the experimental and computational results: the maximum difference between experimental and computational is 2˚C for probe 1, over the temperature range of 25˚C to 53˚C.

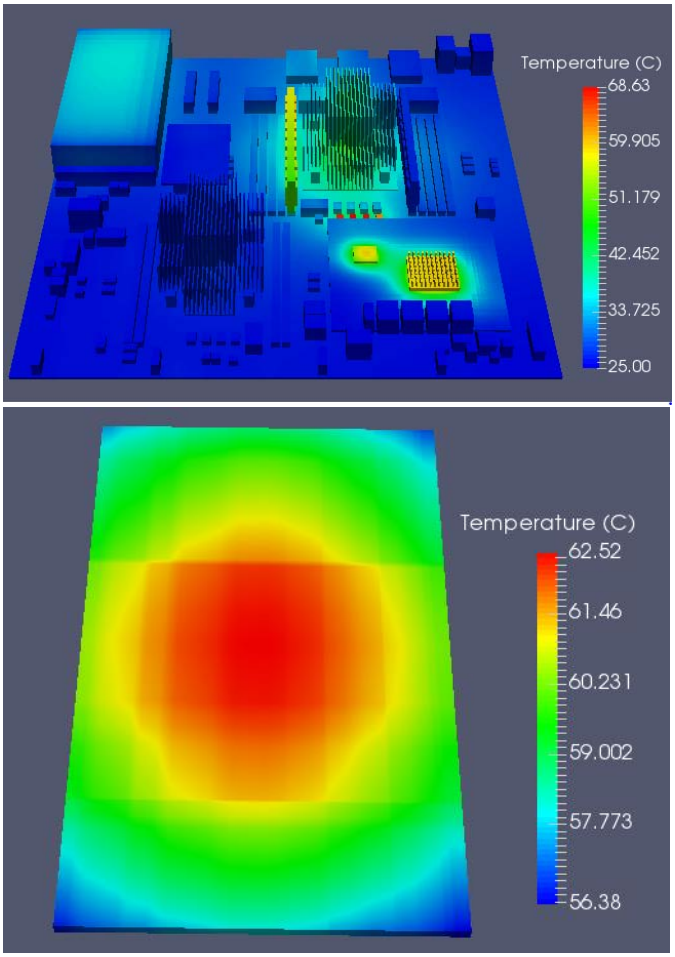


Figure 8 CFD simulation result: temperature distribution (Top) and IC1 die temperature distribution (Bottom)

In the measurement only surface temperature of different positions is measured and in the CFD simulator, temperature inside the chip is also detected. According to the present results comparison, the temperature difference of experimental and computational results is acceptable.

The CFD steady-state simulation takes almost three hours in the current scenario which is slow for this kind of large case. Next we will examine the aforementioned thermal circuit simulator and make a comparative analysis between them in section 4.4.

4.4 Network-based thermal simulation

In the thermal model extraction, all solid parts of the computer server are divided into the motherboard, 2 packages, one daughterboard, one power board and many other components etc. Note, some of the insignificant components are ignored in the system thermal simulation. Fig.9 shows the entire thermal model network assembly for the computer server after solid and fluid extractions.

In this thermal explorer simulator, both steady-state and transient simulations can be done under different conditions. For steady state, when the server works in the maximum power consumption. The simulation time for this case is 16 to 20 minutes using network-based thermal simulator, which is much less time than CFD simulator. Note that the thermal simulator need to call CFD data.

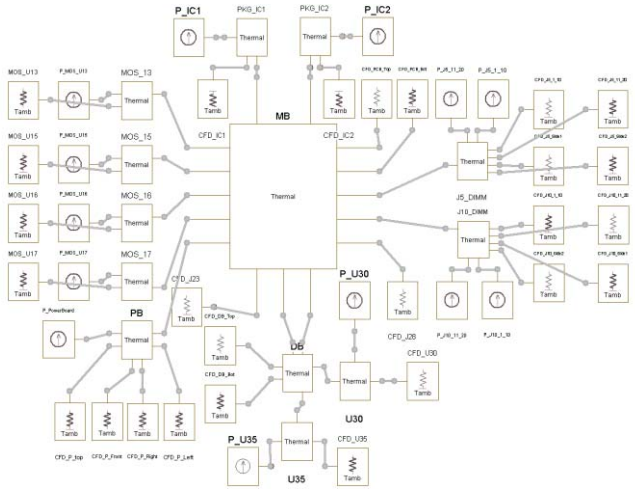


Figure 9. Thermal model network assembly for computer server

In steady-state thermal simulation, as Table 6 shows, making a comparison between the measured and thermal network simulated results: the maximum difference is less than 1.5˚C for probe 1, and for Probe 2, the temperature difference value is less than 2.5 ˚C. Overall the steady state results are matched well between the simulation and measurement.

Table 6: Measured and thermal model simulated temperature of different power dissipation.

Temp	P1-31W	P2-41.8W	P3-64.5W	P4-82.4W
Probe1				
Measurement	35.02 ºC	39.10 ºC	46.86 ºC	53.00 ºC
Thermal Model	36.40 ºC	40.39 ºC	47.94 ºC	54.31 ºC
ΔT_Probe1	**-1.38 ºC**	**-1.29 ºC**	**-1.08 ºC**	**-1.31 ºC**
Probe2				
Measurement	30.60 ºC	30.70 ºC	34.55 ºC	35.75 ºC
Thermal Model	30.11 ºC	31.74 ºC	35.18 ºC	37.89 ºC
ΔT_Probe2	**0.49 ºC**	**-1.04 ºC**	**-0.63 ºC**	**-2.14 ºC**

Table 7 compares the temperature results from the CFD simulator and the network-based thermal simulator when IC1 works in the maximum power dissipation. The steady-state temperature difference obtained by the two simulators in the current scenario is about 3-5ºC, which is acceptable. Also, the CFD simulation results are lower than the network-based thermal simulator.

Table 7 Simulated IC1 package temperature from the CFD simulator and the network-based thermal simulator

Max Temp	CFD	Thermal Circuit	△T
IC1-Die	62.52 ºC	66.70 ºC	-4.18 ºC
PKG-Top	51.18 ºC	54.54 ºC	-3.36 ºC

For transient simulations, we setup the chip power consumption in different service states according to the proceeding transient measurements in section 4.2. The rising and falling time of the input power sources in the simulation is based on the estimated time from the measurement. We tried our best to make these setup values as close to reality as possible, but inevitable there will be some errors from the test setup that are not modeled properly.

Fig.10 shows the transient simulation results of IC1 Die (Red line) and Caps temperature (Lower lines). That the simulation results show the maximum temperature of the Die is about 12˚C higher than the package shell. This is consistent with the previous CFD simulation. The maximum temperature of the Die obtained by CFD simulator is 11.3˚C higher than that of the package shell.

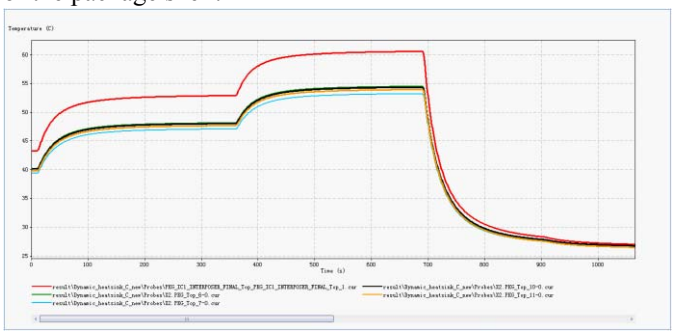


Figure 10 Transient simulation results

In contrast to the measured temperature in section 4.2, the simulated transient results of the IC1 package shell（probe 1）, as shown in Fig.11, the simulation and measurement results match well when the power is on, but simulated temperature drops much faster than the measured results when the power is reset. In the measurements, some energy might be dissipated from the thermocouples which inevitably causes the transient measurements to become sluggish and slower than simulated. In addition, the difference in the temperature transient rates may also be caused by the material properties especially the mass density and specific heat. For probe 2 (PCB top near IC1), the simulation and measurement results match well in the time range under different power dissipation.

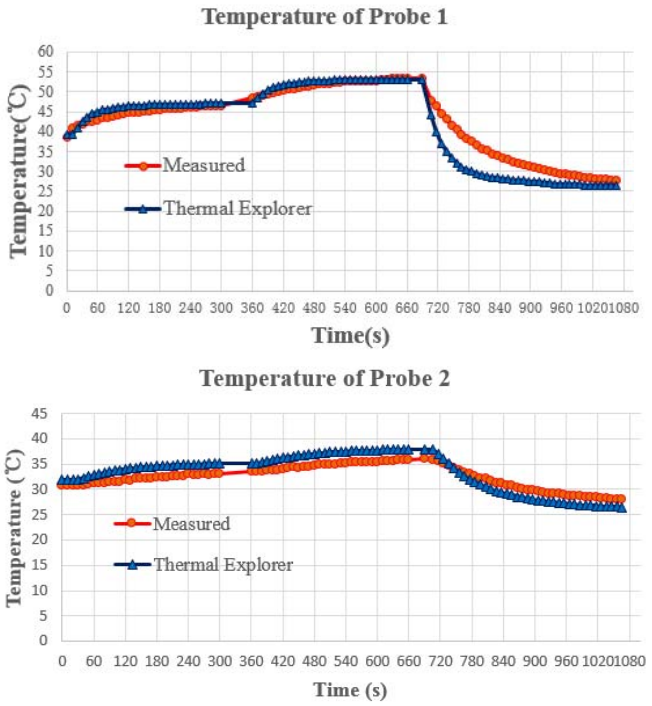


Figure 11 Measured and Thermal Explorer simulated transient results of IC1 package shell(Probe1) and PCB top near IC1(Probe2)

Overall the steady state results and the time-variation trends match well between the simulation and measurement.

5. Conclusion

In Huawei's computer server product, we have done experimental and computational studies. Comparative results show that the temperature difference of simulated and measured results is less than 4.5^{o}C and it meets the product design requirements. Further research and verification will continue in future products.

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